## Features

- Utilizes the AVR® RISC Architecture
- AVR – High-performance and Low-power RISC Architecture
  - 120 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
- Data and Non-volatile Program and Data Memories
  - 2K Bytes of In-System Self Programmable Flash
    Endurance 10,000 Write/Erase Cycles
  - 128 Bytes In-System Programmable EEPROM
    Endurance: 100,000 Write/Erase Cycles
  - 128 Bytes Internal SRAM
  - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes
  - Four PWM Channels
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with On-chip Oscillator
  - USI – Universal Serial Interface
  - Full Duplex USART
- Special Microcontroller Features
  - debugWIRE On-chip Debugging
  - In-System Programmable via SPI Port
  - External and Internal Interrupt Sources
  - Low-power Idle, Power-down, and Standby Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - 18 Programmable I/O Lines
  - 20-pin PDIP, 20-pin SOIC, 20-pad QFN/MLF
- Operating Voltages
  - 1.8 – 5.5V (ATtiny2313V)
  - 2.7 – 5.5V (ATtiny2313)
- Speed Grades
  - ATtiny2313V: 0 – 4 MHz @ 1.8 - 5.5V, 0 – 10 MHz @ 2.7 – 5.5V
  - ATtiny2313: 0 – 10 MHz @ 2.7 - 5.5V, 0 – 20 MHz @ 4.5 – 5.5V
- Typical Power Consumption
  - Active Mode
    1 MHz, 1.8V: 230 µA
    32 kHz, 1.8V: 20 µA (including oscillator)
  - Power-down Mode
    < 0.1 µA at 1.8V

# 8-bit AVR® Microcontroller with 2K Bytes In-System Programmable Flash

# ATtiny2313/V

# Preliminary

# Summary

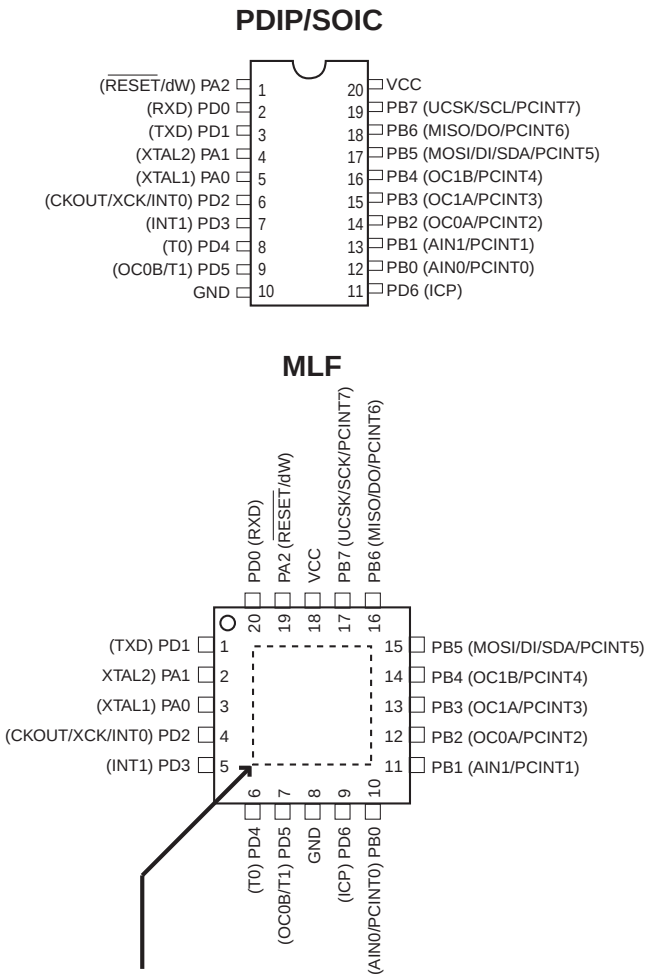
Not recommended for new designs. Use:

– ATtiny2313A

Rev. 2543JS–AVR–11/09

## Pin Configurations

**Figure 1.** Pinout ATtiny2313



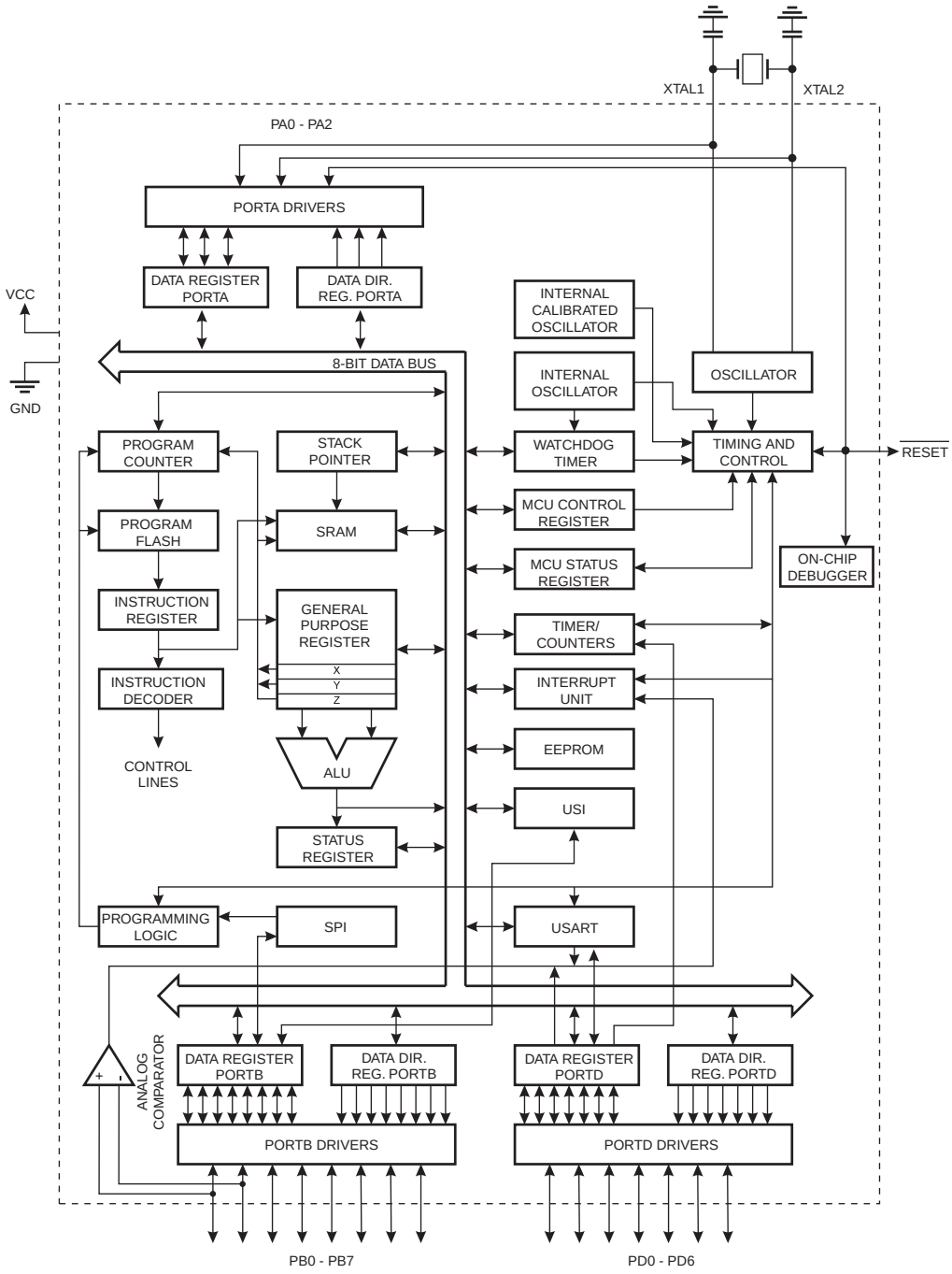

NOTE: Bottom pad should be soldered to ground.

## Overview

The ATtiny2313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

## Block Diagram

**Figure 2.** Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATtiny2313 provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, 18 general purpose I/O lines, 32 general purpose working registers, a single-wire Interface for On-chip Debugging, two flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, a programmable Watchdog Timer with internal Oscillator, and three software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Standby mode, the crystal/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

The device is manufactured using Atmel's high density non-volatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, or by a conventional non-volatile memory programmer. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATtiny2313 is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny2313 AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

## Pin Descriptions

**VCC** Digital supply voltage.

**GND** Ground.

**Port A (PA2..PA0)** Port A is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny2313 as listed on page 55.

**Port B (PB7..PB0)** Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny2313 as listed on page 55.

**Port D (PD6..PD0)** Port D is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATtiny2313 as listed on page 58.

**$\overline{\text{RESET}}$** Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in Table 15 on page 36. Shorter pulses are not guaranteed to generate a reset. The Reset Input is an alternate function for PA2 and dW.

**XTAL1** Input to the inverting Oscillator amplifier and input to the internal clock operating circuit. XTAL1 is an alternate function for PA0.

**XTAL2** Output from the inverting Oscillator amplifier. XTAL2 is an alternate function for PA1.

## Resources

A comprehensive set of development tools, application notes and datasheets are available for downloadon http://www.atmel.com/avr.

## About Code Examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

## Disclaimer

Typical values contained in this data sheet are based on simulations and characterization of other AVR microcontrollers manufactured on the same process technology. Min and Max values will be available after the device is characterized.

## Register Summary

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Page |
|---|---|---|---|---|---|---|---|---|---|---|
| 0x3F (0x5F) | SREG | I | T | H | S | V | N | Z | C | 10 |
| 0x3E (0x5E) | Reserved | – | – | – | – | – | – | – | – | |
| 0x3D (0x5D) | SPL | SP7 | SP6 | SP5 | SP4 | SP3 | SP2 | SP1 | SP0 | 13 |
| 0x3C (0x5C) | OCR0B | Timer/Counter0 – Compare Register B | | | | | | | | 79 |
| 0x3B (0x5B) | GIMSK | INT1 | INT0 | PCIE | – | – | – | – | – | 62 |
| 0x3A (0x5A) | EIFR | INTF1 | INTF0 | PCIF | – | – | – | – | – | 63 |
| 0x39 (0x59) | TIMSK | TOIE1 | OCIE1A | OCIE1B | – | ICIE1 | OCIE0B | TOIE0 | OCIE0A | 80, 111 |
| 0x38 (0x58) | TIFR | TOV1 | OCF1A | OCF1B | – | ICF1 | OCF0B | TOV0 | OCF0A | 80 |
| 0x37 (0x57) | SPMCSR | – | – | – | CTPB | RFLB | PGWRT | PGERS | SELFPRGEN | 157 |
| 0x36 (0x56) | OCR0A | Timer/Counter0 – Compare Register A | | | | | | | | 79 |
| 0x35 (0x55) | MCUCR | PUD | SM1 | SE | SM0 | ISC11 | ISC10 | ISC01 | ISC00 | 55 |
| 0x34 (0x54) | MCUSR | – | – | – | – | WDRF | BORF | EXTRF | PORF | 39 |
| 0x33 (0x53) | TCCR0B | FOC0A | FOC0B | – | – | WGM02 | CS02 | CS01 | CS00 | 78 |
| 0x32 (0x52) | TCNT0 | Timer/Counter0 (8-bit) | | | | | | | | 79 |
| 0x31 (0x51) | OSCCAL | – | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | 28 |
| 0x30 (0x50) | TCCR0A | COM0A1 | COM0A0 | COM0B1 | COM0B0 | – | – | WGM01 | WGM00 | 75 |
| 0x2F (0x4F) | TCCR1A | COM1A1 | COM1A0 | COM1B1 | COM1BO | – | – | WGM11 | WGM10 | 106 |
| 0x2E (0x4E) | TCCR1B | ICNC1 | ICES1 | – | WGM13 | WGM12 | CS12 | CS11 | CS10 | 109 |
| 0x2D (0x4D) | TCNT1H | Timer/Counter1 – Counter Register High Byte | | | | | | | | 110 |
| 0x2C (0x4C) | TCNT1L | Timer/Counter1 – Counter Register Low Byte | | | | | | | | 110 |
| 0x2B (0x4B) | OCR1AH | Timer/Counter1 – Compare Register A High Byte | | | | | | | | 110 |
| 0x2A (0x4A) | OCR1AL | Timer/Counter1 – Compare Register A Low Byte | | | | | | | | 110 |
| 0x29 (0x49) | OCR1BH | Timer/Counter1 – Compare Register B High Byte | | | | | | | | 111 |
| 0x28 (0x48) | OCR1BL | Timer/Counter1 – Compare Register B Low Byte | | | | | | | | 111 |
| 0x27 (0x47) | Reserved | – | – | – | – | – | – | – | – | |
| 0x26 (0x46) | CLKPR | CLKPCE | – | – | – | CLKPS3 | CLKPS2 | CLKPS1 | CLKPS0 | 30 |
| 0x25 (0x45) | ICR1H | Timer/Counter1 - Input Capture Register High Byte | | | | | | | | 111 |
| 0x24 (0x44) | ICR1L | Timer/Counter1 - Input Capture Register Low Byte | | | | | | | | 111 |
| 0x23 (0x43) | GTCCR | – | – | – | – | – | – | – | PSR10 | 83 |
| 0x22 (0x42) | TCCR1C | FOC1A | FOC1B | – | – | – | – | – | – | 110 |
| 0x21 (0x41) | WDTCSR | WDIF | WDIE | WDP3 | WDCE | WDE | WDP2 | WDP1 | WDP0 | 44 |
| 0x20 (0x40) | PCMSK | PCINT7 | PCINT6 | PCINT5 | PCINT4 | PCINT3 | PCINT2 | PCINT1 | PCINT0 | 63 |
| 0x1F (0x3F) | Reserved | – | – | – | – | – | – | – | – | |
| 0x1E (0x3E) | EEAR | – | EEPROM Address Register | | | | | | | 18 |
| 0x1D (0x3D) | EEDR | EEPROM Data Register | | | | | | | | 19 |
| 0x1C (0x3C) | EECR | – | – | EEPM1 | EEPM0 | EERIE | EEMPE | EEPE | EERE | 19 |
| 0x1B (0x3B) | PORTA | – | – | – | – | – | PORTA2 | PORTA1 | PORTA0 | 60 |
| 0x1A (0x3A) | DDRA | – | – | – | – | – | DDA2 | DDA1 | DDA0 | 60 |
| 0x19 (0x39) | PINA | – | – | – | – | – | PINA2 | PINA1 | PINA0 | 60 |
| 0x18 (0x38) | PORTB | PORTB7 | PORTB6 | PORTB5 | PORTB4 | PORTB3 | PORTB2 | PORTB1 | PORTB0 | 60 |
| 0x17 (0x37) | DDRB | DDB7 | DDB6 | DDB5 | DDB4 | DDB3 | DDB2 | DDB1 | DDB0 | 60 |
| 0x16 (0x36) | PINB | PINB7 | PINB6 | PINB5 | PINB4 | PINB3 | PINB2 | PINB1 | PINB0 | 60 |
| 0x15 (0x35) | GPIOR2 | General Purpose I/O Register 2 | | | | | | | | 23 |
| 0x14 (0x34) | GPIOR1 | General Purpose I/O Register 1 | | | | | | | | 23 |
| 0x13 (0x33) | GPIOR0 | General Purpose I/O Register 0 | | | | | | | | 23 |
| 0x12 (0x32) | PORTD | – | PORTD6 | PORTD5 | PORTD4 | PORTD3 | PORTD2 | PORTD1 | PORTD0 | 60 |
| 0x11 (0x31) | DDRD | – | DDD6 | DDD5 | DDD4 | DDD3 | DDD2 | DDD1 | DDD0 | 60 |
| 0x10 (0x30) | PIND | – | PIND6 | PIND5 | PIND4 | PIND3 | PIND2 | PIND1 | PIND0 | 60 |
| 0x0F (0x2F) | USIDR | USI Data Register | | | | | | | | 146 |
| 0x0E (0x2E) | USISR | USISIF | USIOIF | USIPF | USIDC | USICNT3 | USICNT2 | USICNT1 | USICNT0 | 147 |
| 0x0D (0x2D) | USICR | USISIE | USIOIE | USIWM1 | USIWM0 | USICS1 | USICS0 | USICLK | USITC | 147 |
| 0x0C (0x2C) | UDR | UART Data Register (8-bit) | | | | | | | | 131 |
| 0x0B (0x2B) | UCSRA | RXC | TXC | UDRE | FE | DOR | UPE | U2X | MPCM | 131 |
| 0x0A (0x2A) | UCSRB | RXCIE | TXCIE | UDRIE | RXEN | TXEN | UCSZ2 | RXB8 | TXB8 | 133 |
| 0x09 (0x29) | UBRRL | UBRRH[7:0] | | | | | | | | 135 |
| 0x08 (0x28) | ACSR | ACD | ACBG | ACO | ACI | ACIE | ACIC | ACIS1 | ACIS0 | 151 |
| 0x07 (0x27) | Reserved | – | – | – | – | – | – | – | – | |
| 0x06 (0x26) | Reserved | – | – | – | – | – | – | – | – | |
| 0x05 (0x25) | Reserved | – | – | – | – | – | – | – | – | |
| 0x04 (0x24) | Reserved | – | – | – | – | – | – | – | – | |
| 0x03 (0x23) | UCSRC | – | UMSEL | UPM1 | UPM0 | USBS | UCSZ1 | UCSZ0 | UCPOL | 134 |
| 0x02 (0x22) | UBRRH | – | – | – | – | UBRRH[11:8] | | | | 135 |
| 0x01 (0x21) | DIDR | – | – | – | – | – | – | AIN1D | AIN0D | 152 |
| 0x00 (0x20) | Reserved | – | – | – | – | – | – | – | – | |

Note:
1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.
2. I/O Registers within the address range 0x00 - 0x1F are directly bit-accessible using the SBI and CBI instructions. In these registers, the value of single bits can be checked by using the SBIS and SBIC instructions.
3. Some of the status flags are cleared by writing a logical one to them. Note that, unlike most other AVRs, the CBI and SBI instructions will only operate on the specified bit, and can therefore be used on registers containing such status flags. The CBI and SBI instructions work with registers 0x00 to 0x1F only.
4. When using the I/O specific commands IN and OUT, the I/O addresses 0x00 - 0x3F must be used. When addressing I/O Registers as data space using LD and ST instructions, 0x20 must be added to these addresses.

# Instruction Set Summary

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| **ARITHMETIC AND LOGIC INSTRUCTIONS** | | | | | |
| ADD | Rd, Rr | Add two Registers | Rd ← Rd + Rr | Z,C,N,V,H | 1 |
| ADC | Rd, Rr | Add with Carry two Registers | Rd ← Rd + Rr + C | Z,C,N,V,H | 1 |
| ADIW | Rdl,K | Add Immediate to Word | Rdh:Rdl ← Rdh:Rdl + K | Z,C,N,V,S | 2 |
| SUB | Rd, Rr | Subtract two Registers | Rd ← Rd - Rr | Z,C,N,V,H | 1 |
| SUBI | Rd, K | Subtract Constant from Register | Rd ← Rd - K | Z,C,N,V,H | 1 |
| SBC | Rd, Rr | Subtract with Carry two Registers | Rd ← Rd - Rr - C | Z,C,N,V,H | 1 |
| SBCI | Rd, K | Subtract with Carry Constant from Reg. | Rd ← Rd - K - C | Z,C,N,V,H | 1 |
| SBIW | Rdl,K | Subtract Immediate from Word | Rdh:Rdl ← Rdh:Rdl - K | Z,C,N,V,S | 2 |
| AND | Rd, Rr | Logical AND Registers | Rd ← Rd • Rr | Z,N,V | 1 |
| ANDI | Rd, K | Logical AND Register and Constant | Rd ← Rd • K | Z,N,V | 1 |
| OR | Rd, Rr | Logical OR Registers | Rd ← Rd v Rr | Z,N,V | 1 |
| ORI | Rd, K | Logical OR Register and Constant | Rd ← Rd v K | Z,N,V | 1 |
| EOR | Rd, Rr | Exclusive OR Registers | Rd ← Rd ⊕ Rr | Z,N,V | 1 |
| COM | Rd | One's Complement | Rd ← 0xFF – Rd | Z,C,N,V | 1 |
| NEG | Rd | Two's Complement | Rd ← 0x00 – Rd | Z,C,N,V,H | 1 |
| SBR | Rd,K | Set Bit(s) in Register | Rd ← Rd v K | Z,N,V | 1 |
| CBR | Rd,K | Clear Bit(s) in Register | Rd ← Rd • (0xFF - K) | Z,N,V | 1 |
| INC | Rd | Increment | Rd ← Rd + 1 | Z,N,V | 1 |
| DEC | Rd | Decrement | Rd ← Rd – 1 | Z,N,V | 1 |
| TST | Rd | Test for Zero or Minus | Rd ← Rd • Rd | Z,N,V | 1 |
| CLR | Rd | Clear Register | Rd ← Rd ⊕ Rd | Z,N,V | 1 |
| SER | Rd | Set Register | Rd ← 0xFF | None | 1 |
| **BRANCH INSTRUCTIONS** | | | | | |
| RJMP | k | Relative Jump | PC ← PC + k + 1 | None | 2 |
| IJMP | | Indirect Jump to (Z) | PC ← Z | None | 2 |
| RCALL | k | Relative Subroutine Call | PC ← PC + k + 1 | None | 3 |
| ICALL | | Indirect Call to (Z) | PC ← Z | None | 3 |
| RET | | Subroutine Return | PC ← STACK | None | 4 |
| RETI | | Interrupt Return | PC ← STACK | I | 4 |
| CPSE | Rd,Rr | Compare, Skip if Equal | if (Rd = Rr) PC ← PC + 2 or 3 | None | 1/2/3 |
| CP | Rd,Rr | Compare | Rd – Rr | Z, N,V,C,H | 1 |
| CPC | Rd,Rr | Compare with Carry | Rd – Rr – C | Z, N,V,C,H | 1 |
| CPI | Rd,K | Compare Register with Immediate | Rd – K | Z, N,V,C,H | 1 |
| SBRC | Rr, b | Skip if Bit in Register Cleared | if (Rr(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBRS | Rr, b | Skip if Bit in Register is Set | if (Rr(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIC | P, b | Skip if Bit in I/O Register Cleared | if (P(b)=0) PC ← PC + 2 or 3 | None | 1/2/3 |
| SBIS | P, b | Skip if Bit in I/O Register is Set | if (P(b)=1) PC ← PC + 2 or 3 | None | 1/2/3 |
| BRBS | s, k | Branch if Status Flag Set | if (SREG(s) = 1) then PC←PC+k + 1 | None | 1/2 |
| BRBC | s, k | Branch if Status Flag Cleared | if (SREG(s) = 0) then PC←PC+k + 1 | None | 1/2 |
| BREQ | k | Branch if Equal | if (Z = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRNE | k | Branch if Not Equal | if (Z = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRCS | k | Branch if Carry Set | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRCC | k | Branch if Carry Cleared | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRSH | k | Branch if Same or Higher | if (C = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLO | k | Branch if Lower | if (C = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRMI | k | Branch if Minus | if (N = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRPL | k | Branch if Plus | if (N = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRGE | k | Branch if Greater or Equal, Signed | if (N ⊕ V= 0) then PC ← PC + k + 1 | None | 1/2 |
| BRLT | k | Branch if Less Than Zero, Signed | if (N ⊕ V= 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHS | k | Branch if Half Carry Flag Set | if (H = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRHC | k | Branch if Half Carry Flag Cleared | if (H = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRTS | k | Branch if T Flag Set | if (T = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRTC | k | Branch if T Flag Cleared | if (T = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRVS | k | Branch if Overflow Flag is Set | if (V = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRVC | k | Branch if Overflow Flag is Cleared | if (V = 0) then PC ← PC + k + 1 | None | 1/2 |
| BRIE | k | Branch if Interrupt Enabled | if ( I = 1) then PC ← PC + k + 1 | None | 1/2 |
| BRID | k | Branch if Interrupt Disabled | if ( I = 0) then PC ← PC + k + 1 | None | 1/2 |
| **BIT AND BIT-TEST INSTRUCTIONS** | | | | | |
| SBI | P,b | Set Bit in I/O Register | I/O(P,b) ← 1 | None | 2 |
| CBI | P,b | Clear Bit in I/O Register | I/O(P,b) ← 0 | None | 2 |
| LSL | Rd | Logical Shift Left | Rd(n+1) ← Rd(n), Rd(0) ← 0 | Z,C,N,V | 1 |
| LSR | Rd | Logical Shift Right | Rd(n) ← Rd(n+1), Rd(7) ← 0 | Z,C,N,V | 1 |
| ROL | Rd | Rotate Left Through Carry | Rd(0)←C,Rd(n+1)← Rd(n),C←Rd(7) | Z,C,N,V | 1 |

| Mnemonics | Operands | Description | Operation | Flags | #Clocks |
|---|---|---|---|---|---|
| ROR | Rd | Rotate Right Through Carry | Rd(7)←C,Rd(n)← Rd(n+1),C←Rd(0) | Z,C,N,V | 1 |
| ASR | Rd | Arithmetic Shift Right | Rd(n) ← Rd(n+1), n=0..6 | Z,C,N,V | 1 |
| SWAP | Rd | Swap Nibbles | Rd(3..0)←Rd(7..4),Rd(7..4)←Rd(3..0) | None | 1 |
| BSET | s | Flag Set | SREG(s) ← 1 | SREG(s) | 1 |
| BCLR | s | Flag Clear | SREG(s) ← 0 | SREG(s) | 1 |
| BST | Rr, b | Bit Store from Register to T | T ← Rr(b) | T | 1 |
| BLD | Rd, b | Bit load from T to Register | Rd(b) ← T | None | 1 |
| SEC | | Set Carry | C ← 1 | C | 1 |
| CLC | | Clear Carry | C ← 0 | C | 1 |
| SEN | | Set Negative Flag | N ← 1 | N | 1 |
| CLN | | Clear Negative Flag | N ← 0 | N | 1 |
| SEZ | | Set Zero Flag | Z ← 1 | Z | 1 |
| CLZ | | Clear Zero Flag | Z ← 0 | Z | 1 |
| SEI | | Global Interrupt Enable | I ← 1 | I | 1 |
| CLI | | Global Interrupt Disable | I ← 0 | I | 1 |
| SES | | Set Signed Test Flag | S ← 1 | S | 1 |
| CLS | | Clear Signed Test Flag | S ← 0 | S | 1 |
| SEV | | Set Twos Complement Overflow. | V ← 1 | V | 1 |
| CLV | | Clear Twos Complement Overflow | V ← 0 | V | 1 |
| SET | | Set T in SREG | T ← 1 | T | 1 |
| CLT | | Clear T in SREG | T ← 0 | T | 1 |
| SEH | | Set Half Carry Flag in SREG | H ← 1 | H | 1 |
| CLH | | Clear Half Carry Flag in SREG | H ← 0 | H | 1 |
| **DATA TRANSFER INSTRUCTIONS** | | | | | |
| MOV | Rd, Rr | Move Between Registers | Rd ← Rr | None | 1 |
| MOVW | Rd, Rr | Copy Register Word | Rd+1:Rd ← Rr+1:Rr | None | 1 |
| LDI | Rd, K | Load Immediate | Rd ← K | None | 1 |
| LD | Rd, X | Load Indirect | Rd ← (X) | None | 2 |
| LD | Rd, X+ | Load Indirect and Post-Inc. | Rd ← (X), X ← X + 1 | None | 2 |
| LD | Rd, - X | Load Indirect and Pre-Dec. | X ← X - 1, Rd ← (X) | None | 2 |
| LD | Rd, Y | Load Indirect | Rd ← (Y) | None | 2 |
| LD | Rd, Y+ | Load Indirect and Post-Inc. | Rd ← (Y), Y ← Y + 1 | None | 2 |
| LD | Rd, - Y | Load Indirect and Pre-Dec. | Y ← Y - 1, Rd ← (Y) | None | 2 |
| LDD | Rd,Y+q | Load Indirect with Displacement | Rd ← (Y + q) | None | 2 |
| LD | Rd, Z | Load Indirect | Rd ← (Z) | None | 2 |
| LD | Rd, Z+ | Load Indirect and Post-Inc. | Rd ← (Z), Z ← Z+1 | None | 2 |
| LD | Rd, -Z | Load Indirect and Pre-Dec. | Z ← Z - 1, Rd ← (Z) | None | 2 |
| LDD | Rd, Z+q | Load Indirect with Displacement | Rd ← (Z + q) | None | 2 |
| LDS | Rd, k | Load Direct from SRAM | Rd ← (k) | None | 2 |
| ST | X, Rr | Store Indirect | (X) ← Rr | None | 2 |
| ST | X+, Rr | Store Indirect and Post-Inc. | (X) ← Rr, X ← X + 1 | None | 2 |
| ST | - X, Rr | Store Indirect and Pre-Dec. | X ← X - 1, (X) ← Rr | None | 2 |
| ST | Y, Rr | Store Indirect | (Y) ← Rr | None | 2 |
| ST | Y+, Rr | Store Indirect and Post-Inc. | (Y) ← Rr, Y ← Y + 1 | None | 2 |
| ST | - Y, Rr | Store Indirect and Pre-Dec. | Y ← Y - 1, (Y) ← Rr | None | 2 |
| STD | Y+q,Rr | Store Indirect with Displacement | (Y + q) ← Rr | None | 2 |
| ST | Z, Rr | Store Indirect | (Z) ← Rr | None | 2 |
| ST | Z+, Rr | Store Indirect and Post-Inc. | (Z) ← Rr, Z ← Z + 1 | None | 2 |
| ST | -Z, Rr | Store Indirect and Pre-Dec. | Z ← Z - 1, (Z) ← Rr | None | 2 |
| STD | Z+q,Rr | Store Indirect with Displacement | (Z + q) ← Rr | None | 2 |
| STS | k, Rr | Store Direct to SRAM | (k) ← Rr | None | 2 |
| LPM | | Load Program Memory | R0 ← (Z) | None | 3 |
| LPM | Rd, Z | Load Program Memory | Rd ← (Z) | None | 3 |
| LPM | Rd, Z+ | Load Program Memory and Post-Inc | Rd ← (Z), Z ← Z+1 | None | 3 |
| SPM | | Store Program Memory | (Z) ← R1:R0 | None | - |
| IN | Rd, P | In Port | Rd ← P | None | 1 |
| OUT | P, Rr | Out Port | P ← Rr | None | 1 |
| PUSH | Rr | Push Register on Stack | STACK ← Rr | None | 2 |
| POP | Rd | Pop Register from Stack | Rd ← STACK | None | 2 |
| **MCU CONTROL INSTRUCTIONS** | | | | | |
| NOP | | No Operation | | None | 1 |
| SLEEP | | Sleep | (see specific descr. for Sleep function) | None | 1 |
| WDR | | Watchdog Reset | (see specific descr. for WDR/timer) | None | 1 |
| BREAK | | Break | For On-chip Debug Only | None | N/A |

## Ordering Information

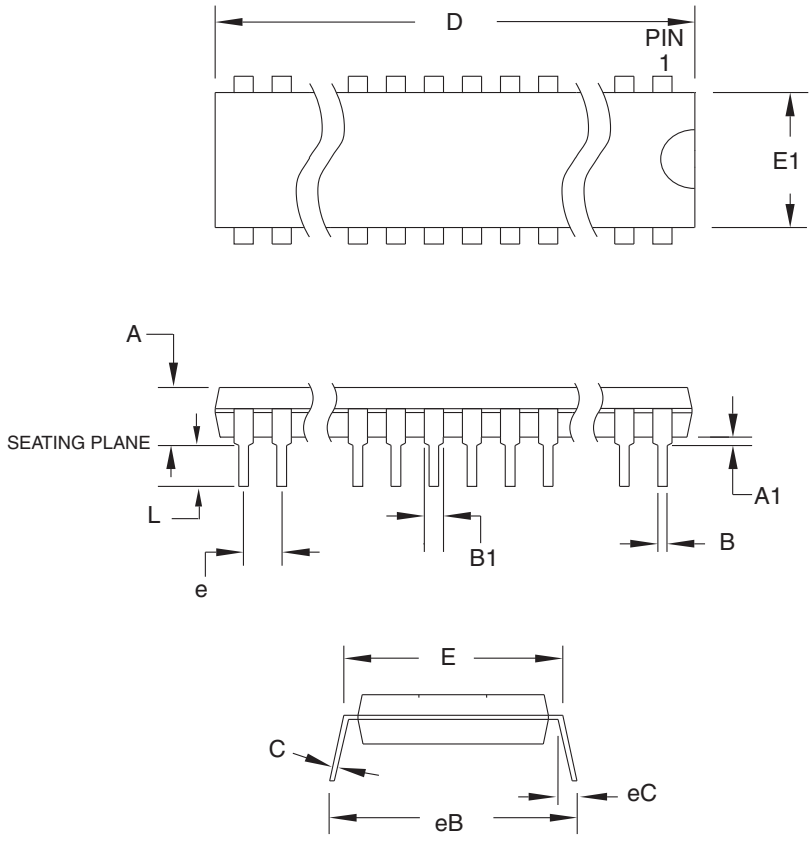
| Speed (MHz)[3] | Power Supply | Ordering Code | Package[1] | Operation Range |
|---|---|---|---|---|
| 10 | 1.8 - 5.5V | ATtiny2313V-10PI<br>ATtiny2313V-10PU[2]<br>ATtiny2313V-10SI<br>ATtiny2313V-10SU[2]<br>ATtiny2313V-10MU[2] | 20P3<br>20P3<br>20S<br>20S<br>20M1 | Industrial<br>(-40°C to 85°C) |
| 20 | 2.7 - 5.5V | ATtiny2313-20PI<br>ATtiny2313-20PU[2]<br>ATtiny2313-20SI<br>ATtiny2313-20SU[2]<br>ATtiny2313-20MU[2] | 20P3<br>20P3<br>20S<br>20S<br>20M1 | Industrial<br>(-40°C to 85°C) |

Note:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging alternative, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive).Also Halide free and fully Green.
3. For Speed vs. $V_{CC,}$ see Figure 82 on page 182 and Figure 83 on page 182.

| Package Type | |
|---|---|
| **20P3** | 20-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| **20S** | 20-lead, 0.300" Wide, Plastic Gull Wing Small Outline Package (SOIC) |
| **20M1** | 20-pad, 4 x 4 x 0.8 mm Body, Quad Flat No-Lead/Micro Lead Frame Package (MLF) |

# Packaging Information

## 20P3




**COMMON DIMENSIONS**
(Unit of Measure = mm)

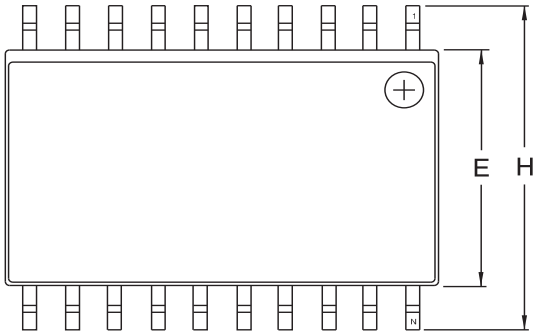
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 5.334 | |
| A1 | 0.381 | – | – | |
| D | 25.493 | – | 25.984 | Note 2 |
| E | 7.620 | – | 8.255 | |
| E1 | 6.096 | – | 7.112 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.270 | – | 1.551 | |
| L | 2.921 | – | 3.810 | |
| C | 0.203 | – | 0.356 | |
| eB | – | – | 10.922 | |
| eC | 0.000 | – | 1.524 | |
| e | 2.540 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-001, Variation AD.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

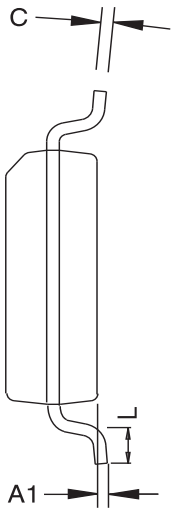
1/12/04

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20P3**, 20-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP) | 20P3 | C |

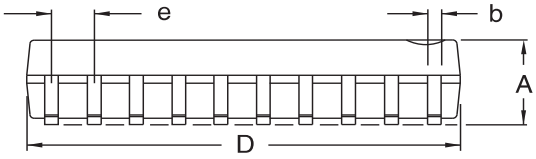
## 20S




Top View




End View




Side View

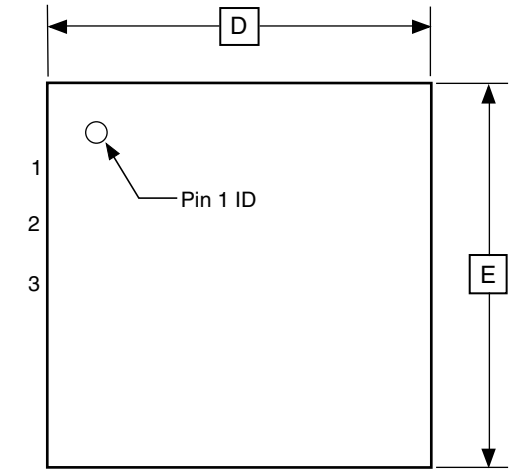
**COMMON DIMENSIONS**
(Unit of Measure – mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 2.35 | | 2.65 | |
| A1 | 0.10 | | 0.30 | |
| b | 0.33 | | 0.51 | 4 |
| C | 0.23 | | 0.32 | |
| D | 12.60 | | 13.00 | 1 |
| E | 7.40 | | 7.60 | 2 |
| H | 10.00 | | 10.65 | |
| L | 0.40 | | 1.27 | 3 |
| e | 1.27 BSC | | | |

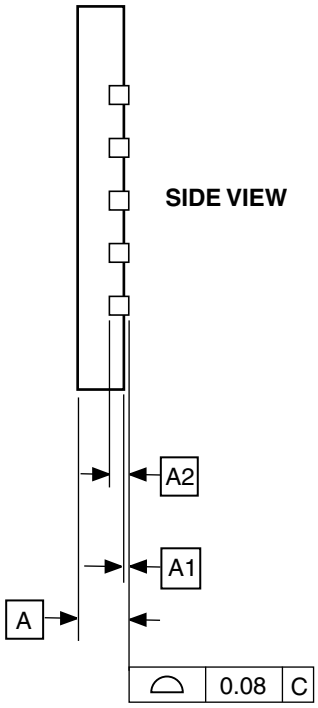
Notes.
1. This drawing is for general information only; refer to JEDEC Drawing MS-013, Variation AC for additional information.
2. Dimension 'D' does not include mold Flash, protrusions or gate burrs. Mold Flash, protrusions and gate burrs shall not exceed 0.15 mm (0.006') per side.
3. Dimension 'E' does not include inter-lead Flash or protrusion. Inter-lead Flash and protrusions shall not exceed 0.25 mm (0.010') per side.
4. 'L' is the length of the terminal for soldering to a substrate.
5. The lead width 'b', as measured 0.36 mm (0.014') or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.024') per side.

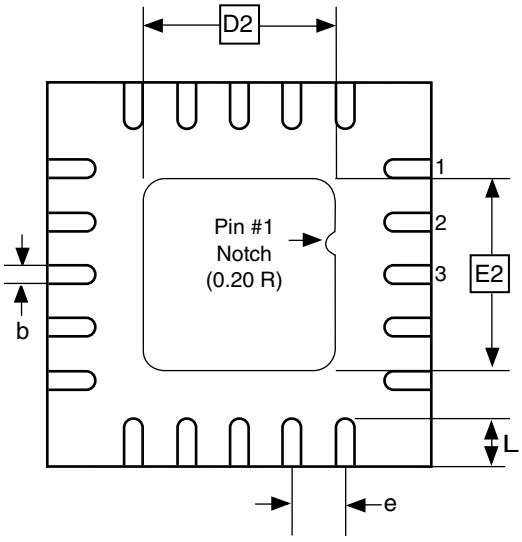
11/6/06

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20S2**, 20-lead, 0.300' Wide Body, Plastic Gull Wing Small Outline Package (SOIC) | 20S2 | B |




TOP VIEW




BOTTOM VIEW

**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 | |
| A1 | – | 0.01 | 0.05 | |
| A2 | | 0.20 REF | | |
| b | 0.18 | 0.23 | 0.30 | |
| D | | 4.00 BSC | | |
| D2 | 2.45 | 2.60 | 2.75 | |
| E | | 4.00 BSC | | |
| E2 | 2.45 | 2.60 | 2.75 | |
| e | | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.55 | |

Note: Reference JEDEC Standard MO-220, Fig. 1 (SAW Singulation) WGGD-5.

10/27/04

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **20M1**, 20-pad, 4 x 4 x 0.8 mm Body, Lead Pitch 0.50 mm,<br>2.6 mm Exposed Pad, Micro Lead Frame Package (MLF) | 20M1 | A |

## Errata

The revision in this section refers to the revision of the ATtiny2313 device.

### ATtiny2313 Rev B

- **Wrong values read after Erase Only operation**
- **Parallel Programming does not work**
- **Watchdog Timer Interrupt disabled**
- **EEPROM can not be written below 1.9 volts**

1. **Wrong values read after Erase Only operation**

   At supply voltages below 2.7 V, an EEPROM location that is erased by the Erase Only operation may read as programmed (0x00).

   **Problem Fix/Workaround**

   If it is necessary to read an EEPROM location after Erase Only, use an Atomic Write operation with 0xFF as data in order to erase a location. In any case, the Write Only operation can be used as intended. Thus no special considerations are needed as long as the erased location is not read before it is programmed.

2. **Parallel Programming does not work**

   Parallel Programming is not functioning correctly. Because of this, reprogramming of the device is impossible if one of the following modes are selected:

   – In-System Programming disabled (SPIEN unprogrammed)

   – Reset Disabled (RSTDISBL programmed)

   **Problem Fix/Workaround**

   Serial Programming is still working correctly. By avoiding the two modes above, the device can be reprogrammed serially.

3. **Watchdog Timer Interrupt disabled**

   If the watchdog timer interrupt flag is not cleared before a new timeout occurs, the watchdog will be disabled, and the interrupt flag will automatically be cleared. This is only applicable in interrupt only mode. If the Watchdog is configured to reset the device in the watchdog time-out following an interrupt, the device works correctly.

   **Problem fix / Workaround**

   Make sure there is enough time to always service the first timeout event before a new watchdog timeout occurs. This is done by selecting a long enough time-out period.

4. **EEPROM can not be written below 1.9 volts**

   Writing the EEPROM at $V_{CC}$ below 1.9 volts might fail.

   **Problem fix / Workaround**

   Do not write the EEPROM when $V_{CC}$ is below 1.9 volts.

### ATtiny2313 Rev A

Revision A has not been sampled.

## Datasheet Revision History

Please note that the referring page numbers in this section are referred to this document. The referring revision in this section are referring to the document revision.

### Rev. J - 11/09

1. Updated template
2. Changed device status to “Not recommended for new designs.”
3. Updated “Stack Pointer” on page 13.
4. Updated Table “Sleep Mode Select” on page 32.
5. Updated “Calibration Byte” on page 162 (to one byte of calibration data)

### Changes from Rev. 2514H-02/05 to Rev. 2514I-04/06

1. Updated typos.
2. Updated Figure 1 on page 2.
3. Added “Resources” on page 6.
4. Updated “Default Clock Source” on page 25.
5. Updated “128 kHz Internal Oscillator” on page 30.
6. Updated “Power Management and Sleep Modes” on page 32
7. Updated Table 3 on page 25,Table 13 on page 32, Table 14 on page 33, Table 19 on page 44, Table 31 on page 62, Table 79 on page 178.
8. Updated “External Interrupts” on page 61.
9. Updated “Bit 7..0 – PCINT7..0: Pin Change Enable Mask 7..0” on page 63.
10. Updated “Bit 6 – ACBG: Analog Comparator Bandgap Select” on page 151.
11. Updated “Calibration Byte” on page 162.
12. Updated “DC Characteristics” on page 179.
13. Updated “Register Summary” on page 9.
14. Updated “Ordering Information” on page 13.
15. Changed occurences of OCnA to OCFnA, OCnB to OCFnB and OC1x to OCF1x.

### Changes from Rev. 2514G-10/04 to Rev. 2514H-02/05

1. Updated Table 6 on page 27, Table 15 on page 36, Table 68 on page 162 and Table 80 on page 181.
2. Changed CKSEL default value in “Default Clock Source” on page 25 to 8 MHz.
3. Updated “Programming the Flash” on page 167, “Programming the EEPROM” on page 169 and “Enter Programming Mode” on page 165.
4. Updated “DC Characteristics” on page 179.
5. MLF option updated to “Quad Flat No-Lead/Micro Lead Frame (QFN/MLF)”

### Changes from Rev. 2514F-08/04 to Rev. 2514G-10/04

1. Updated “Features” on page 1.
2. Updated “Pinout ATtiny2313” on page 2.

3. Updated "Ordering Information" on page 13.
4. Updated "Packaging Information" on page 14.
5. Updated "Errata" on page 17.

### Changes from Rev. 2514E-04/04 to Rev. 2514F-08/04

1. Updated "Features" on page 1.
2. Updated "Alternate Functions of Port B" on page 55.
3. Updated "Calibration Byte" on page 162.
4. Moved Table 69 on page 162 and Table 70 on page 162 to "Page Size" on page 162.
5. Updated "Enter Programming Mode" on page 165.
6. Updated "Serial Programming Algorithm" on page 175.
7. Updated Table 78 on page 176.
8. Updated "DC Characteristics" on page 179.
9. Updated "ATtiny2313 Typical Characteristics" on page 183.
10. Changed occurences of PCINT15 to PCINT7, EEMWE to EEMPE and EEWE to EEPE in the document.

### Changes from Rev. 2514D-03/04 to Rev. 2514E-04/04

1. Speed Grades changed
   - 12MHz to 10MHz
   - 24MHz to 20MHz
2. Updated Figure 1 on page 2.
3. Updated "Ordering Information" on page 13.
4. Updated "Maximum Speed vs. $V_{CC}$" on page 182.
5. Updated "ATtiny2313 Typical Characteristics" on page 183.

### Changes from Rev. 2514C-12/03 to Rev. 2514D-03/04

1. Updated Table 2 on page 25.
2. Replaced "Watchdog Timer" on page 41.
3. Added "Maximum Speed vs. $V_{CC}$" on page 182.
4. "Serial Programming Algorithm" on page 175 updated.
5. Changed mA to µA in preliminary Figure 136 on page 209.
6. "Ordering Information" on page 13 updated.
   MLF package option removed
7. Package drawing "20P3" on page 14 updated.
8. Updated C-code examples.
9. Renamed instances of SPMEN to SELFPRGEN, Self Programming Enable.

### Changes from Rev. 2514B-09/03 to Rev. 2514C-12/03

1. Updated "Calibrated Internal RC Oscillator" on page 27.

### Changes from Rev. 2514A-09/03 to Rev. 2514B-09/03

1. Fixed typo from UART to USART and updated Speed Grades and Power Consumption Estimates in "Features" on page 1.
2. Updated "Pin Configurations" on page 2.
3. Updated Table 15 on page 36 and Table 80 on page 181.
4. Updated item 5 in "Serial Programming Algorithm" on page 175.
5. Updated "Electrical Characteristics" on page 179.
6. Updated Figure 82 on page 182 and added Figure 83 on page 182.
7. Changed SFIOR to GTCCR in "Register Summary" on page 9.
8. Updated "Ordering Information" on page 13.
9. Added new errata in "Errata" on page 17.

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