Features

- High Performance RF-CMOS 2.4 GHz Radio Transceiver Targeted for IEEE 802.15.4 and ZigBee Applications
- Industry Leading Link Budget (104 dB):
  - Programmable Output Power from -17 dBm up to 3 dBm
  - Receiver Sensitivity -101 dBm
- Ultra-Low Power Consumption:
  - SLEEP: 0.1 µA
  - RX: 16 mA
  - TX: 17 mA (at max Transmit Power of 3 dBm)
- Ultra-Low Supply Voltage (1.8V to 3.6V) with Internal Regulator
- Optimized for Low BoM Cost and Ease of Production:
  - Few External Components Necessary (Crystal, Capacitors and Antenna)
  - Excellent ESD Robustness
- Easy to Use Interface:
  - Registers and Frame Buffer Accessible through Fast SPI
  - Only Two Microcontroller GPIO Lines Necessary
  - One Interrupt Pin from Radio Transceiver
  - Clock Output with Prescaler from Radio Transceiver
- Radio Transceiver Features:
  - 128-byte SRAM for Data Buffering
  - Programmable Clock Output, to Clock the Host Microcontroller or as Timer Reference
  - Integrated TX/RX Switch
  - Fully Integrated PLL with on-chip Loop Filter
  - Fast PLL Settling Time
  - Battery Monitor
  - Fast Power-Up Time < 1 ms
- Special IEEE 802.15.4-2003 Hardware Support:
  - FCS Computation
  - Clear Channel Assessment
  - Energy Detection / RSSI Computation
  - Automatic CSMA-CA
  - Automatic Address Filtering
  - Automatic Acknowledge
- Industrial Temperature Range:
  - -40°C to 85°C
- I/O and Packages:
  - 32-pin Low-Profile QFN
  - RoHS/Fully Green
- Compliant to EN 300 328/440, FCC-CFR-47 Part 15, ARIB STD-66, RSS-210
- Compliant to IEEE 802.15.4-2003

ZigBee™ IEEE 802.15.4™ Radio Transceiver

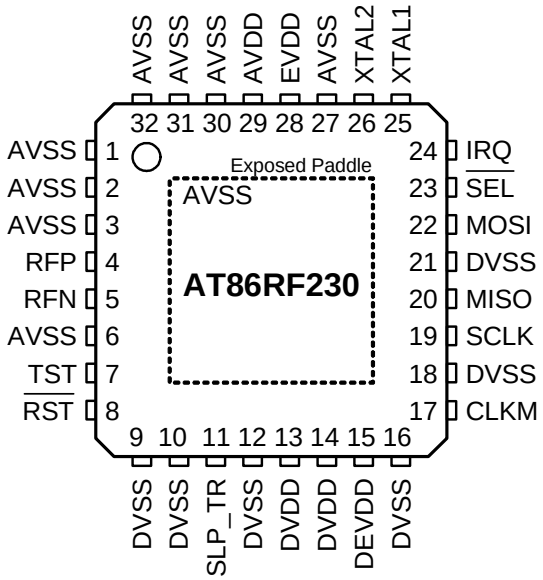
AT86RF230

PRELIMINARY

5131C-ZIGB-05/22/07

1 Pin-out Diagram

Figure 1-1. AT86RF230 Pin-Out Diagram



Note: The exposed paddle is electrically connected to the die inside the package. It shall be soldered to the board to ensure electrical and thermal contact and good mechanical stability.

Disclaimer

Typical values contained in this datasheet are based on simulations and testing. Min and Max values will be available when the radio transceiver has been fully characterized.

2 Overview

The AT86RF230 is a low-power 2.4 GHz radio transceiver especially designed for low cost ZigBee/IEEE 802.15.4-2003 applications. The AT86RF230 is a true SPI-to-antenna solution. All RF-critical components except the antenna, crystal and de-coupling capacitors are integrated on-chip. Therefore, the AT86RF230 is particularly suitable for final applications like:

- Wireless sensor networks
- Industrial control
- Home and building automation
- Consumer electronics
- PC peripherals

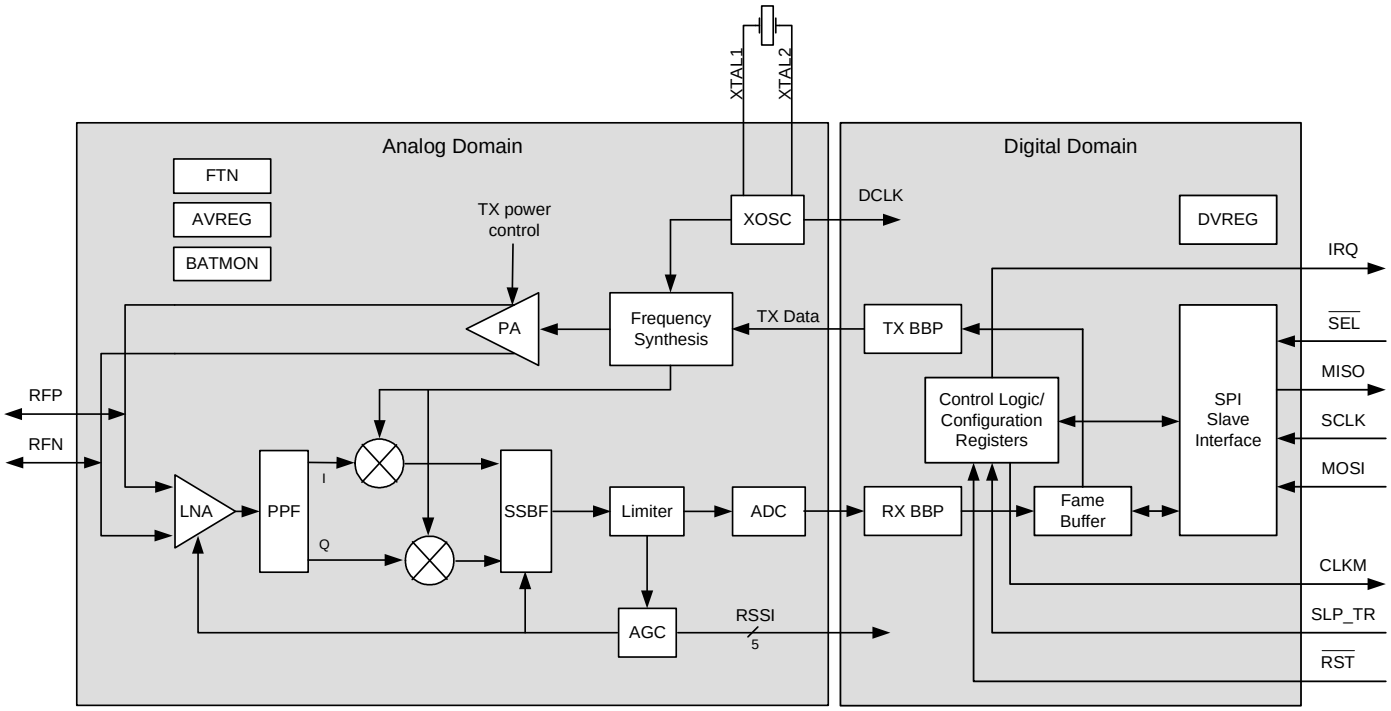
The AT86RF230 can be operated by using an external microcontroller like ATMEL's AVR microcontrollers. A comprehensive software programming description can be found in the application note AVR2001 "AT86RF230 - Software Programmer's Guide".

3 General Circuit Description

This single-chip radio transceiver provides a complete radio transceiver interface between the antenna and the microcontroller. It comprises the analog radio transceiver and digital demodulation including time and frequency synchronization and data buffering. The number of external components is minimized such that only an antenna, a crystal and four decoupling capacitors are required. The bidirectional differential antenna pins are used for RX and TX, so that no external antenna switch is needed.

The AT86RF230 block diagram is shown in **Figure 3-1**.

Figure 3-1. Block Diagram of the AT86RF230



The receiver path is based on a low-IF architecture. The channel filter consists of a single sideband active RC resonator forming a 2 MHz band-pass filter with a Butterworth characteristic centered at 2 MHz. Two 1st-order high-pass filters are added to the signal path to achieve capacitive coupling at the single side-band filter (SSBF) output to suppress DC offset at the limiter amplifier. The limiter amplifier provides sufficient gain to overcome the DC offset of the succeeding ADC and generates a digital RSSI signal with 3 dB granularity. The low-IF signal is sampled at 16 MHz and is applied to the baseband digital signal processor.

On the transmit side, direct VCO modulation is used. The modulation scheme is offset-QPSK (O-QPSK) with half-sine pulse shaping and 32-length block coding (spreading). This is equivalent to minimum shift keying (MSK) when transforming the spreading code sequences appropriately. The modulation signal is passed to the fractional-N PLL generating a coherent phase modulation required for O-QPSK demodulation. The frequency-modulated LO signal is fed to the power amplifier.

Two on-chip low-dropout (LDO) voltage regulators provide the internal analog and digital 1.8V supply. The SPI interface and the control registers retain their settings in SLEEP state (see section 7) when the regulators are turned off.

4 Pin Description

Table 4-1. AT86RF230 Pin List

Number	Name	Type	Description
1	AVSS	Ground	Analog ground
2	AVSS	Ground	Analog ground
3	AVSS	Ground	Ground for RF signals
4	RFP	RF I/O	Differential RF signal
5	RFN	RF I/O	Differential RF signal
6	AVSS	Ground	Ground for RF signals
7	TST	Digital input	Enables Continuous Transmission Test Mode; active high
8	$\overline{\text{RST}}$	Digital input	Chip reset; active low
9	DVSS	Ground	Digital ground
10	DVSS	Ground	Digital ground
11	SLP_TR	Digital input	Controls sleep, transmit start and receive states; active high
12	DVSS	Ground	Digital ground
13	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
14	DVDD	Supply	Regulated 1.8V supply voltage; digital domain
15	DEVDD	Supply	External supply voltage; digital domain
16	DVSS	Ground	Digital ground
17	CLKM	Digital output	Master clock signal output
18	DVSS	Ground	Digital ground
19	SCLK	Digital input	SPI clock
20	MISO	Digital output	SPI data output (master input slave output)
21	DVSS	Ground	Digital ground
22	MOSI	Digital input	SPI data input (master output slave input)
23	$\overline{\text{SEL}}$	Digital input	SPI select; active low
24	IRQ	Digital output	Interrupt request signal; active high
25	XTAL1	Analog input	Crystal pin or external clock supply
26	XTAL2	Analog input	Crystal pin
27	AVSS	Ground	Analog ground
28	EVDD	Supply	External supply voltage; analog domain
29	AVDD	Supply	Regulated 1.8V supply voltage; analog domain
30	AVSS	Ground	Analog ground
31	AVSS	Ground	Analog ground
32	AVSS	Ground	Analog ground
Paddle	AVSS	Ground	Analog ground; Exposed Paddle of QFN package

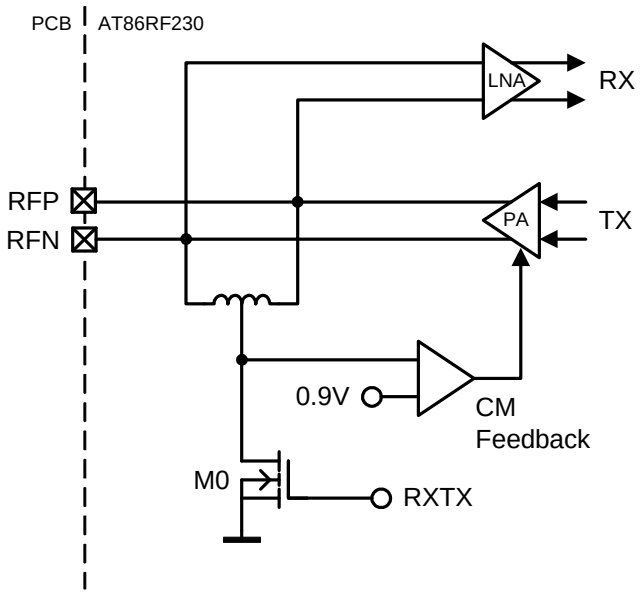
4.1 Analog and RF Pins

A differential RF port (RFP / RFN) provides common-mode rejection to suppress the switching noise of the internal digital signal processing blocks. At the board-level, the differential RF layout ensures high receiver sensitivity by rejecting any spurious interspersions originating from other digital ICs such as the microcontroller.

The RF port is designed for a 100Ω differential load. A DC path between the RF pins is allowed. A DC path to ground or supply voltage is not allowed. Therefore, when connecting a RF-load providing a DC path to the power supply or to ground, capacitive coupling is required as indicated in Table 4-2.

A simplified schematic of the RF front end is shown in **Figure 4-1**.

Figure 4-1. Simplified RF Front-End Schematic



RF port DC values depend on the operating mode. In TRX_OFF state (see section 7), the RF pins are pulled to ground, preventing a floating voltage larger than 1.8V which is not allowed for the internal circuitry. In receive mode, the RF input provides a low-impedance path to ground when transistor M0 (see **Figure 4-1**) pulls the inductor center tap to ground. A DC voltage drop of 20 mV across the on-chip inductor can be measured at the RF pins.

In transmit mode, a control loop provides a common-mode voltage of 0.9V. Transistor M0 is off, allowing the PA to set the common-mode voltage. The common-mode capacitance at each pin to ground shall be < 30 pF to ensure the stability of this common-mode feedback loop.

The internal voltage regulators and the AVDD/DVDD pin configuration are described in section 8.8. A detailed description of the crystal oscillator and the related XTAL1/XTAL2 pin configuration can be found in section 8.10.

Table 4-2. Comments on Analog and RF Pins

Pin	Condition	Recommendation/Comment
RFP/RFN	V_{DC} = 0.9V (TX) V_{DC} = 20 mV (RX) at both pins	AC-coupling is required if an antenna with a DC path to ground is used. Serial capacitance must be < 30 pF.
XTAL1/XTAL2	C_{PAR} = 3 pF V_{DC} = 0.9V at both pins	Parasitic capacitance of the pins (C_{PAR}) must be considered as additional load capacitance to the crystal.
AVDD/DVDD	V_{DC} = 1.8V	Supply pins (voltage regulator outputs) for the analog and digital 1.8V domain. The outputs shall bypassed by 1 µF.

4.2 Digital Pins

4.2.1 Driver Strength Settings

The driver strength of the digital output pins (MISO, IRQ) and CLKM pin can be configured in register 0x03 (TRX_CTRL_0) as described in Table 4-3.

The capacitive load should be as small as possible and not larger than 50 pF when using the 2 mA minimum driver strength setting. Generally, the output driver strength should be adjusted to the lowest possible value in order to keep the current consumption and the emission of digital signal harmonics low.

Table 4-3. Digital Output Driver Configuration

Pin	Default Driver Strength	Comment
MISO, IRQ	2 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA
CLKM	4 mA	Adjustable to 2 mA, 4 mA, 6 mA and 8 mA

4.2.2 Pull-up and Pull-down Configuration

Pulling resistors are connected to all digital input pins in radio transceiver state P_ON (see Section 7). Table 4-4 summarizes the pull-up and pull-down configuration.

Table 4-4. Pull-Up / Pull-Down Configuration of Digital Input Pins in P_ON State

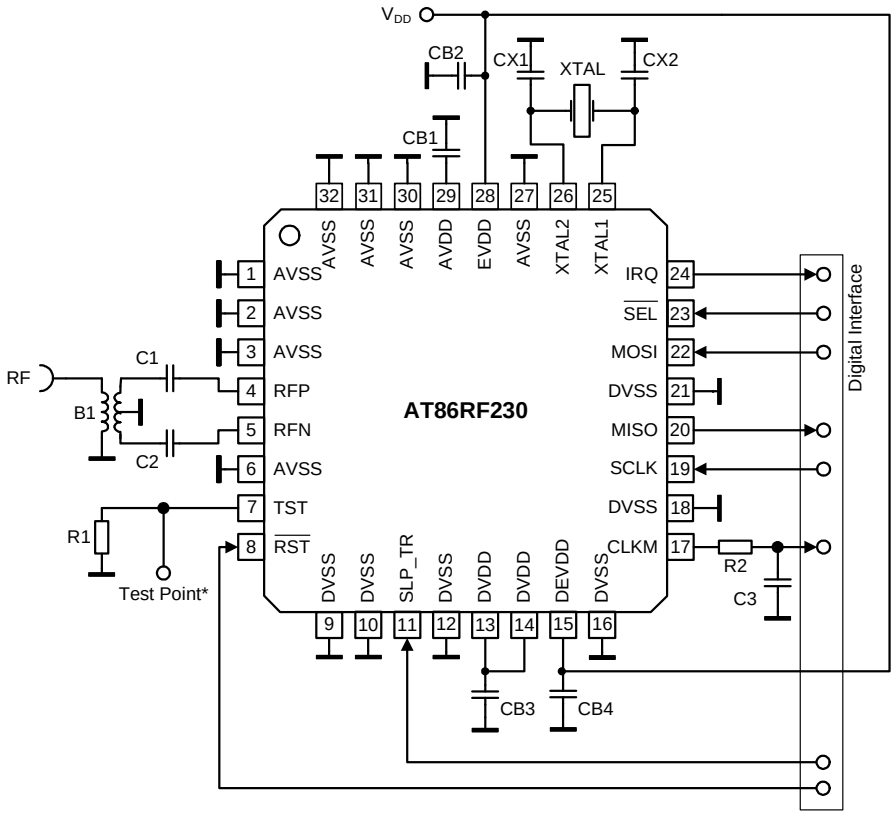
Pin	H = pull-up, L = pull-down
$\overline{RST}$	H
$\overline{SEL}$	H
SCLK	L
MOSI	L
SLP_TR	L

In all other states, no pull-up or pull-down resistors are connected to any of the digital input pins.

5 Application Circuit

An application circuit with a single-ended RF connector is shown in **Figure 5-1**. The balun B1 transforms the 100Ω differential RF port (RFP / RFN) of the AT86RF230 to a 50Ω single-ended RF port. The capacitors C1 and C2 provide AC coupling of the RF signals to the RF pins.

Figure 5-1. Application Circuit Schematic, * for Further Details See “Appendix A - Continuous Transmission Test Mode”



Power supply decoupling capacitors (CB2, CB4) are connected to the external analog supply pin (EVDD pin 28) and the external digital supply pin (DEVDD pin 15). Capacitors CB1 and CB3 are bypass capacitors for the integrated analog and digital voltage regulators to ensure stable operation (1 µF recommended value). All decoupling and bypass capacitors should be placed as close as possible to the AT86RF230 pins and should have a low-resistance and low-inductance connection to ground to achieve the best performance.

The crystal (XTAL), the two load capacitors (CX1, CX2), and the internal circuitry connected to pins XTAL1 and XTAL2 form the crystal oscillator. To achieve the best accuracy and stability of the reference frequency, large parasitic capacitances should be avoided. Crystal lines should be routed as short as possible and not in proximity of digital I/O signals.

Crosstalk from digital signals on the crystal pins or the RF pins can degrade system performance. Therefore, a low-pass filter (C3, R2) is placed close to the CLKM output pin to reduce the radiation of signal harmonics. This is not needed if the CLKM pin is not used and turned off during device initialization.

The application board ground plane should be separated into four independent fragments, the analog, the digital, the antenna and the XTAL ground plane. The exposed paddle shall act as reference of the individual grounds.

For further details see application note AVR2005 "AT86RF230 - Hardware Design Considerations"

Table 5-1. Example Bill of Materials

Designator	Description	Value	Manufacturer	Part Number	Comment
B1	SMD balun	2.4 GHz	Wuerth	748421245	
CB1	LDO VREG bypass capacitor	1 µF	AVX Murata	0603YD105KAT2A GRM188R61C105KA12D	X5R 10% 16V (0603)
CB2	Power supply decoupling	1 µF			
CB3	LDO VREG bypass capacitor	1 µF			
CB4	Power supply decoupling	1 µF			
CX1	Crystal load capacitor	12 pF	AVX Murata	06035A120JA GRP1886C1H120JA01	COG 5% 50V (0603)
CX2	Crystal load capacitor	12 pF			
C1	RF coupling capacitor	22 pF	Epcos Epcos AVX	B37930 B37920 06035A220JAT2A	C0G 5% 50V (0402 or 0603)
C2	RF coupling capacitor	22 pF			
C3	CLKM low-pass filter capacitor	2.2 pF	AVX Murata	06035A229DA GRP1886C1H2R0DA01	COG ±0.5 pF 50V (0603) Designed for f_{CLKM} = 1 MHz
R1	Pull-down resistor	10 kΩ			Recommended 0Ω, if continuous transmission is not required
R2	CLKM low-pass filter resistor	680Ω			Designed for f_{CLKM} = 1 MHz
XTAL	Crystal	CX-4025 16 MHz SX-4025 16 MHz	ACAL Taitjen Siward	XWBBPL-F-1 A207-011	

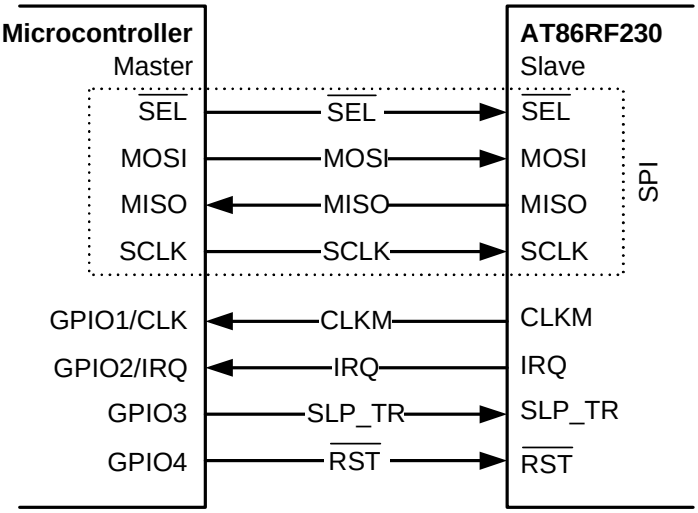
6 Microcontroller Interface

This section describes the AT86RF230 to microcontroller interface. The interface comprises a slave SPI and additional control signals, see **Figure 6-1**. The SPI timing and protocol are described.

Microcontrollers with a master SPI such as Atmel's AVR family interface directly to the AT86RF230. The SPI is used for Frame Buffer and register access. The additional control signals are connected to the GPIO/IRQ interface of the microcontroller.

CLKM can be used as a microcontroller clock source. In this case, the SPI operates in synchronous mode, otherwise in asynchronous mode.

Figure 6-1. Microcontroller to AT86RF230 Interface



6.1 SPI Timing Description

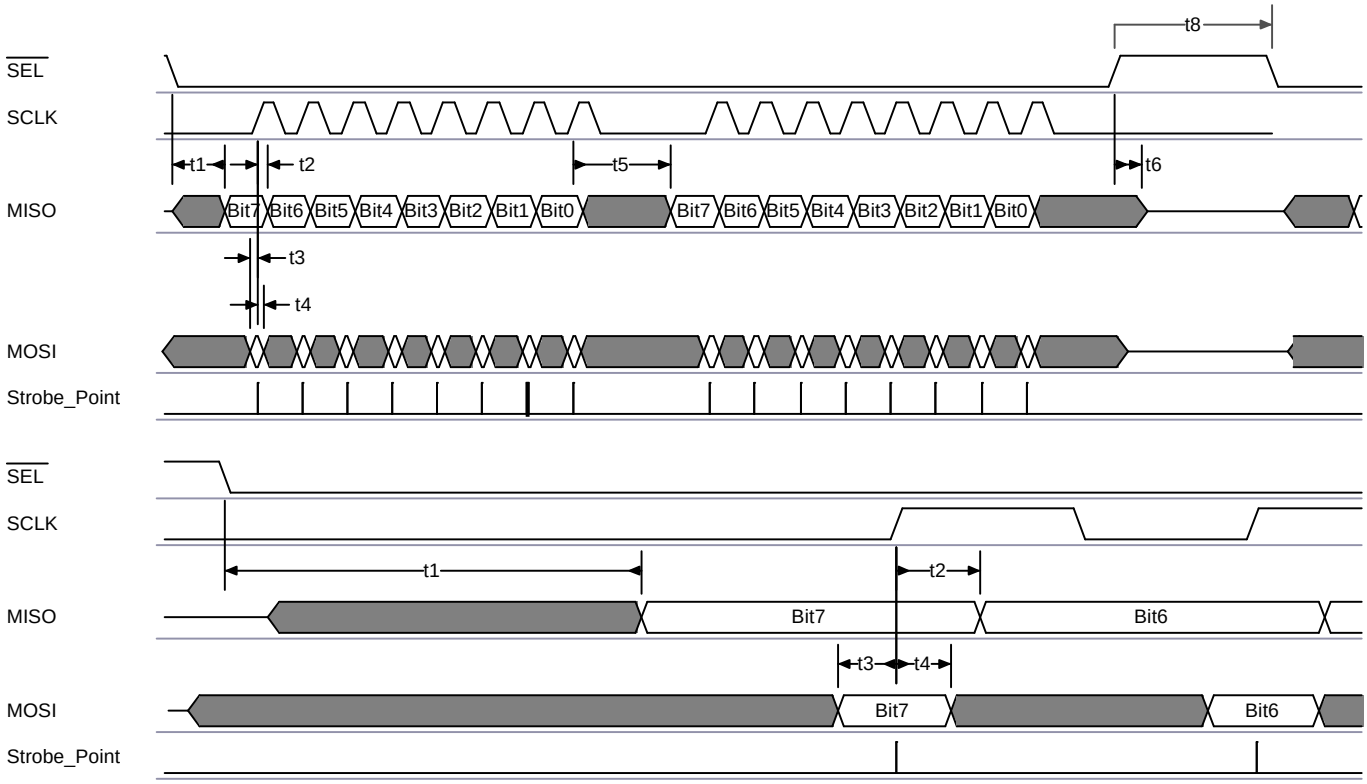
The SPI is designed to work in synchronous or asynchronous mode.

In synchronous mode, the CLKM output of the radio transceiver is used as the master clock of the microcontroller. In this case the maximum SPI clock frequency is 8 MHz.

In asynchronous mode, the maximum SPI clock rate is limited to 7.5 MHz. The signal at pin CLKM is not required and may be disabled.

Figure 6-2 illustrates the SPI timing and introduces its parameters. The corresponding parameter definition is given in Table 9-4.

Figure 6-2. SPI Timing (Upper: Global Map; Lower: Detail Drawing of Timing Parameters t1 to t4)



$\overline{SEL}$ = L enables the MISO output driver of the AT86RF230. If the driver is disabled, there is no internal pull-up resistor connected to it. Driving the appropriate signal level must be ensured by the master device or an external pull-up resistor.

The SPI is a byte-oriented protocol. All bytes are transferred MSB first. During the entire SPI transfer the $\overline{SEL}$ must be logic low. One SPI access sequence includes two or more bytes, depending on the access mode described in Section 6.2.

A SPI communication is always bidirectional. The SPI master starts the transfer by asserting $\overline{SEL}$ = L. The master generates eight SPI clock cycles to transfer a byte to the radio transceiver (via MOSI). At the same time the slave transmits one byte to the master (via MISO). When the master wants to receive one byte of data from the slave it must also transmit one byte to the slave.

Referring to **Figure 6-2**, Strobe_Point indicates the sampling time of MOSI.

6.2 SPI Protocol

Each transfer sequence starts with a command byte from SPI master via MOSI (see Table 6-1). This command byte defines the access mode and additional mode-dependent information. During command byte transfer, the AT86RF230 returns a byte containing 0.

Table 6-1. SPI Command Byte Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Mode
1	0	Register address [5:0]						Register Access Mode – Read Access
1	1	Register address [5:0]						Register Access Mode – Write Access
0	0	1	Reserved					Frame Receive Mode
0	1	1	Reserved					Frame Transmit Mode
0	0	0	Reserved					SRAM Access Mode – Read Access
0	1	0	Reserved					SRAM Access Mode – Write Access

The different access modes are described within the following sections.

6.2.1 Register Access Mode

The Register Access Mode is a two-byte read/write operation. The first byte is the command byte (mode identifier bit 7 = 1, read/write select bit 6, and a 6-bit address). The second byte contains the register read or register write data.

Figure 6-3. Packet Structure - Register Access Mode

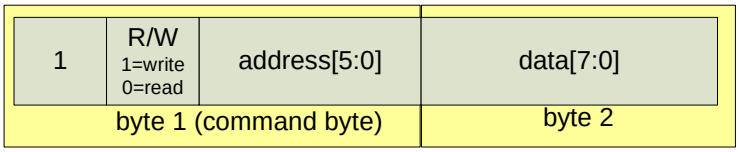
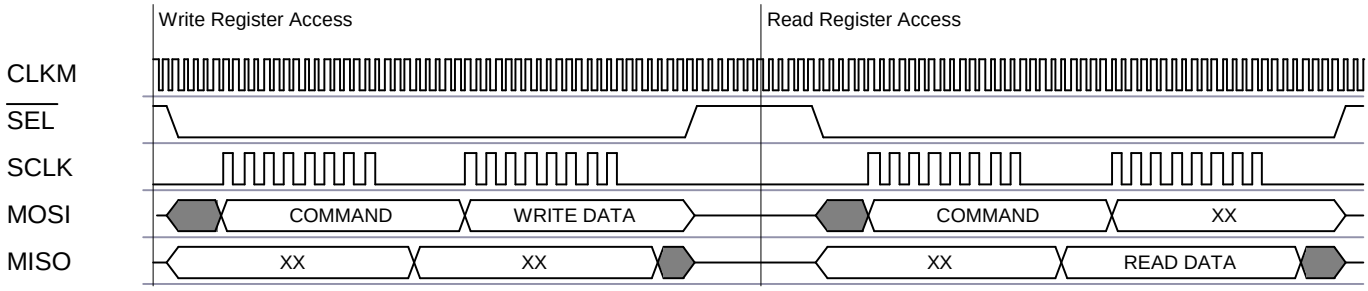


Figure 6-4. Example SPI Sequence - Register Access Mode



6.2.2 Frame Buffer Access Modes

The internal 128-byte Frame Buffer can hold one TX or one RX frame of maximum length at a time. This allows a very flexible data rate over the SPI interface.

The Frame Receive Mode and the Frame Transmit Modes are used to upload or download frames to the microcontroller. Each transfer starts with a command byte. If this byte indicates a frame upload or download, the next byte indicates the frame length followed by the PSDU data (see section 8.3.2). In any receive state, after the PSDU data has been received, one more byte is attached, containing LQI information.

The number of bytes *n* for one frame access is calculated as follow:

Receive: n = 3 + frame_length

[command byte, frame length byte, data, …, LQI byte]

Transmit: n = 2 + frame_length

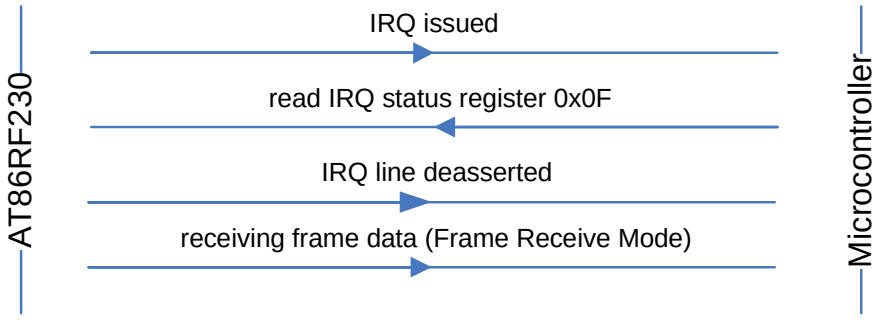
[command byte, frame length byte, data, …]

The maximum value of frame_length is 127 bytes. That means that $n \leq 130$ for Frame Receive Mode and $n \leq 129$ for Frame Transmit Mode.

6.2.2.1 Frame Receive Mode

The transactions required to upload a received frame from the Frame Buffer to the microcontroller are described in **Figure 6-5**. The corresponding SPI timing diagram is shown in **Figure 6-7**.

Figure 6-5. Frame Receive Transactions Between AT86RF230 and Microcontroller



The issued interrupt (see **Figure 6-5**) can be an RX_START or a TRX_END. Waiting for TRX_END before uploading the frame is recommended for operations considered to be none time critical.

Critical protocol timing could require starting the frame upload as soon as possible. The first byte of the frame data can be read 32 µs after the RX_START interrupt. The microcontroller must ensure to read slower than the frame is received. Otherwise, the Frame Buffer will under run and the frame data are not valid. The LQI byte can be uploaded 32 µs after the TRX_END interrupt.

Figure 6-6. Packet Structure - Frame Receive Mode

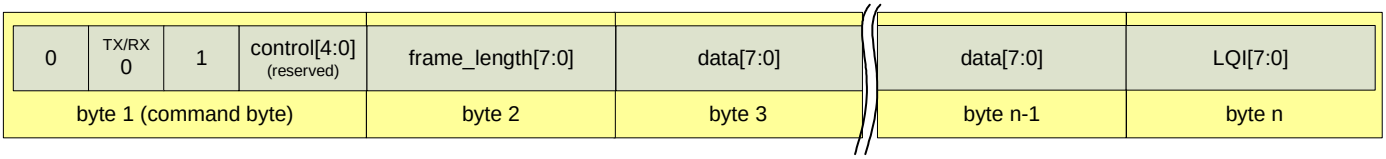
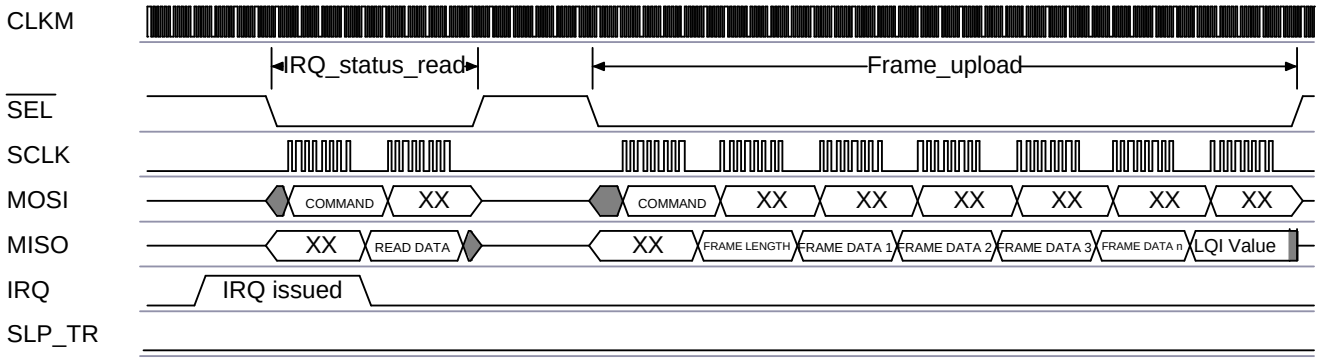


Figure 6-7. Frame Receive Sequence of a 4-byte Payload Frame



6.2.2.2 Frame Transmit Mode

There are two ways to initiate a frame transmission.

The first one is shown in **Figure 6-8** and **Figure 6-10**. In this case a frame transmission is initiated after the completion of the frame download.

Figure 6-8. Frame Transmit Transactions Between AT86RF230 and Microcontroller

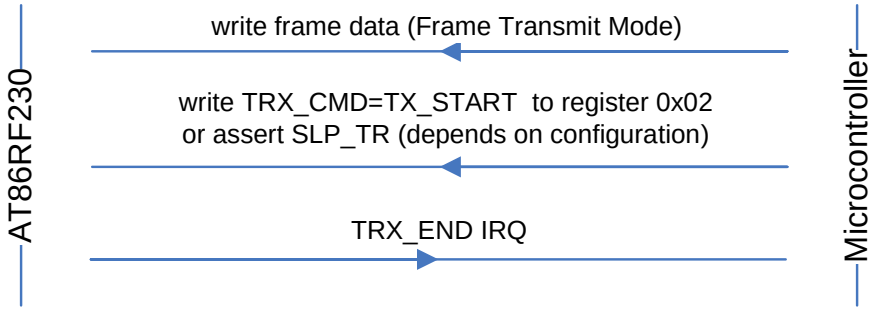


Figure 6-9. Packet Structure - Frame Transmit Mode

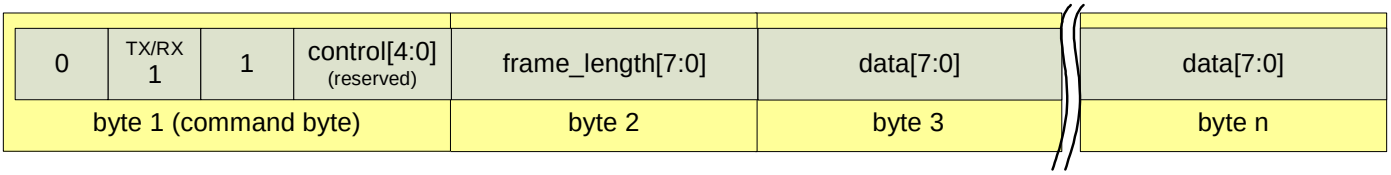
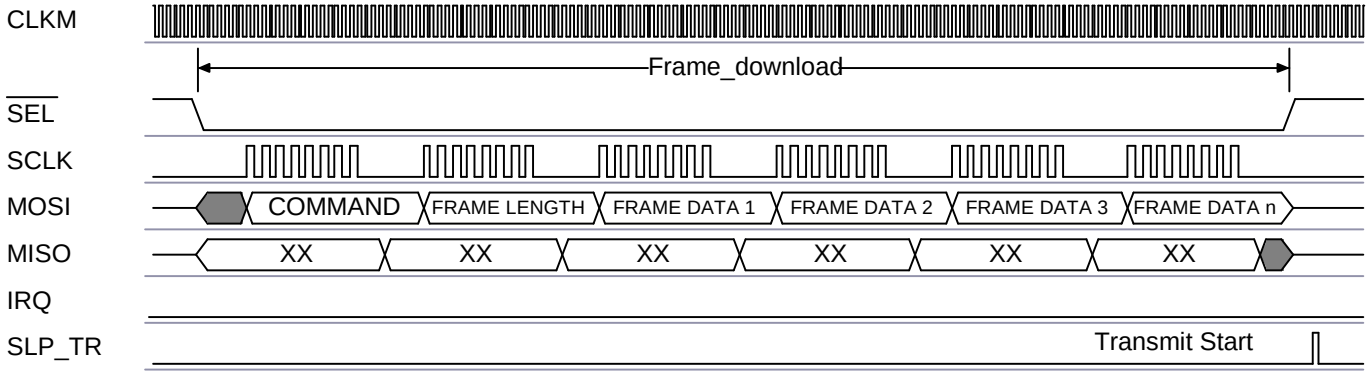
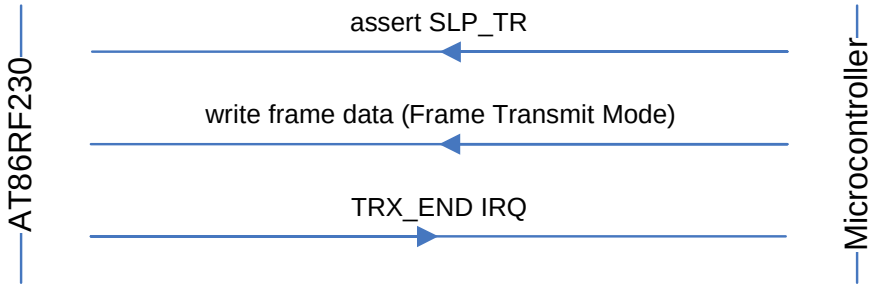


Figure 6-10. Frame Transmit Sequence of a 4-byte Payload Frame (SLP_TR Rising Edge Starts Transmission)



The second method is to start first the frame transmission followed by the frame data download as described in **Figure 6-11**. This is useful for time critical applications. At the rising edge of SPL_TR, the radio transceiver starts transmitting the preamble and the SFD field, which takes about 176 µs. The first byte of the PSDU must be available in the Frame Buffer before this time. The SPI data rate must be higher than 250 kBit/s to ensure that no Frame Buffer under run occurs (TRX_UR IRQ).

Figure 6-11. Time Optimized Frame Transmit Transactions Between AT86RF230 and Microcontroller



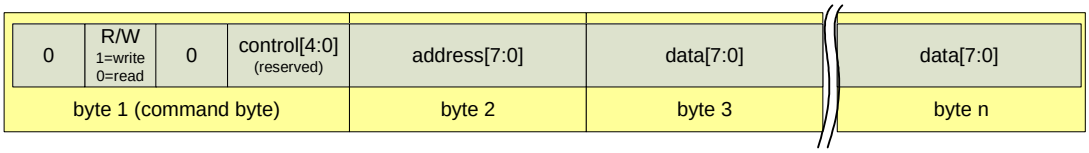
6.2.3 SRAM Access Mode

The SRAM Access Mode allows access to certain bytes within the Frame Buffer. This may reduce SPI traffic.

The SRAM Access Mode is useful, for instance, if a transmit frame is already stored in the Frame Buffer and certain bytes (e.g. sequence number, address field) need to be replaced before retransmitting the frame. Furthermore, it can be used to access the LQI value after frame reception.

If the command byte indicates SRAM Access Mode, the next byte contains the start address. As long as $\overline{\text{SEL}}$ is low, every subsequent byte read or write increments the address counter of the Frame Buffer.

Figure 6-12. Packet Structure - SRAM Access Mode



Notes:

- Because the Frame Buffer is shared between TX and RX, the frame data are overwritten by new incoming frames. If the TX frame data is to be retransmitted, it must be ensured that no frame was received in the meantime.
- If the SRAM Access Mode is used to upload received frames, the Frame Buffer contains all frame data except the frame length byte. The frame length information can be accessed only in the Frame Receive Mode.
- This mode is not intended to be used as an alternative to the Frame Buffer Access Modes (see section 6.2.2).
- It is not possible to transmit received frames without an up and download to the microcontroller.

6.3 Sleep/Wake-up and Transmit Signal (SLP_TR)

The SLP_TR signal is a multi-functional pin. Its function relates to the current state of the AT86RF230 and is summarized in Table 6-2. The radio transceiver states are explained in detail in section 7.

Table 6-2. SLP_TR Multi-Functional Pin

Radio Transceiver Status	Function	Description
TRX_OFF	Sleep	Forces the radio transceiver into SLEEP state
SLEEP	Wakeup	Forces the radio transceiver into TRX_OFF state
RX_ON	Disable CLKM	Forces the radio transceiver into RX_ON_NOCLK state and disables CLKM
RX_AACK_ON	Disable CLKM	Forces the radio transceiver into RX_AACK_ON_NOCLK state and disables CLKM
PLL_ON	TX start	Starts frame transmission
TX_ARET_ON	TX start	Starts of TX_ARET transaction

If used as a sleep signal, releasing pin SLP_TR forces the radio transceiver into TRX_OFF state and enables the main clock. If used as a transmit start signal, the rising edge starts the transmission.

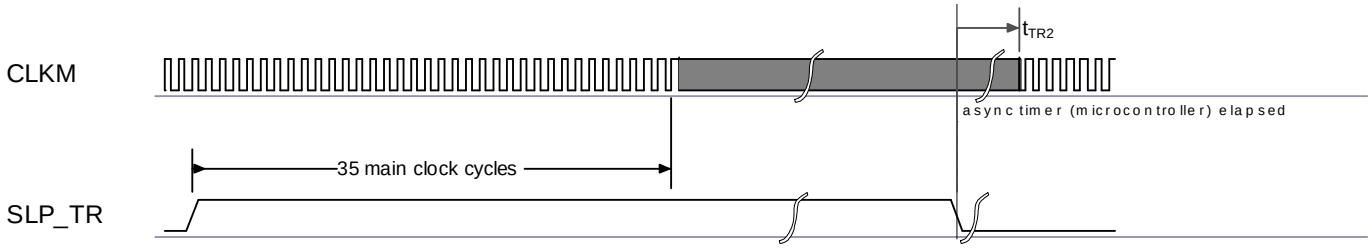
There are two power-down scenarios supported by the AT86RF230 with respect to SLP_TR pin:

- The microcontroller and the radio transceiver are powered down.
- The radio transceiver listens for an incoming frame and the microcontroller is powered down (RX_ON_NOCLK, RX_AACK_ON_NOCLK, BUSY_RX_AACK_NOCLK states).

The first power-down scenario is shown in **Figure 6-13**. The microcontroller forces the AT86RF230 to SLEEP state by setting SLP_TR = H when the radio transceiver is in TRX_OFF

state. The main clock at pin CLKM is switched off after 35 clock cycles. This enables the microcontroller to complete its power-down routine and prevent dead-lock situations. The AT86RF230 awakes when the microcontroller releases the SLP_TR pin. This concept provides the lowest possible power consumption.

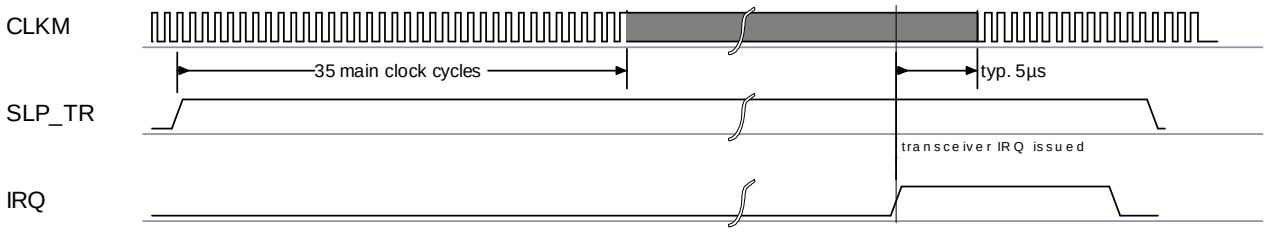
Figure 6-13. Sleep and Wake-up Initiated by Asynchronous Microcontroller Timer Output (for Timing Information See Table 7-3)



Secondly, if an incoming frame is expected and no other application is running on the microcontroller, the microcontroller can be powered down without missing incoming frames. This scenario is shown in **Figure 6-14**. In RX_ON state, the CLKM pin is switched off after 35 clock cycles when setting the pin SLP_TR = H. The radio transceiver state changes to RX_ON_NOCLK. The start of a frame reception is indicated by an RX_START interrupt and the clock is switched on again.

The current consumption of the radio transceiver is similar in state RX_ON_NOCLK / RX_AACK_ON_NOCLK and state RX_ON, because only the CLKM output is switched off.

Figure 6-14. Wake-Up Initiated by Radio Transceiver Interrupt



6.4 Interrupt Logic

6.4.1 Overview

The AT86RF230 can differentiate between six interrupt events. Each interrupt can be enabled or disabled by writing the corresponding bit to the interrupt mask register 0x0E (IRQ_MASK). Internally, each interrupt is stored as a separate bit of the interrupt status register. All interrupt lines are combined via logical “OR” to one external interrupt line. If the external interrupt line is set, the microcontroller must read the interrupt status register 0x0F (IRQ_STATUS) to determine the source of the interrupt. A read access to this register clears the interrupt status register and the external interrupt line, as well. The interrupts are not cleared automatically when the event that caused the IRQ is not valid anymore. Exception: the PLL_LOCK IRQ clears the PLL_UNLOCK IRQ and vice versa. The supported interrupts are summarized in Table 6-3.

Table 6-3. Interrupt Description in Basic Operating Mode

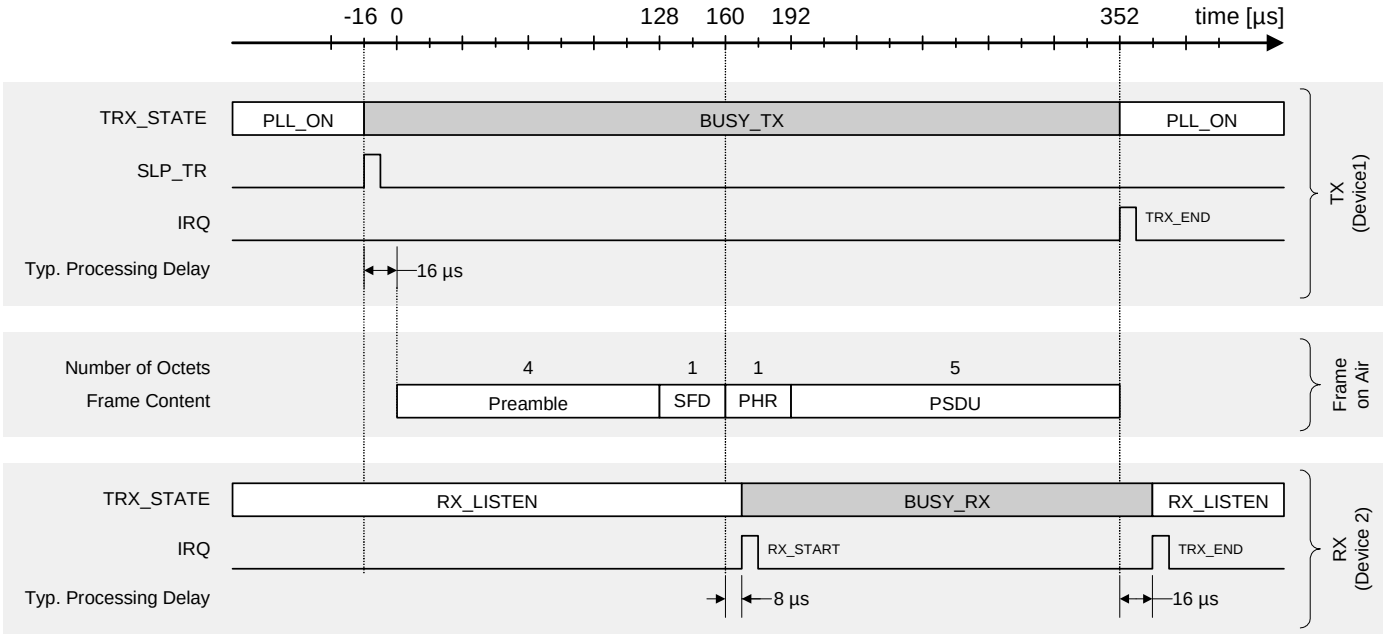
IRQ Register Bit	IRQ Name	Comments
7	IRQ_7: BAT_LOW	Indicates a supply voltage below the programmed threshold.
6	IRQ_6: TRX_UR	Indicates a Frame Buffer access violation.
3	IRQ_3: TRX_END	RX: Indicates the completion of a frame reception. TX: Indicates the completion of a frame transmission.
2	IRQ_2: RX_START	Indicates a SFD detection. The TRX_STATE changes to BUSY_RX.
1	IRQ_1: PLL_UNLOCK	Indicates PLL unlock. The PA is turned off immediately, if the radio transceiver is in BUSY_TX / BUSY_TX_ARET state.
0	IRQ_0: PLL_LOCK	Indicates PLL lock

The interrupt handling in Extended Operating Mode is described in section 7.2.2.

6.4.2 Timing - RX_START and TRX_END Interrupts

Figure 6-15 shows a receive and transmit transaction and the related interrupt events in Basic Operating Mode (see section 7). Processing delays are typical values.

Figure 6-15. Timing of RX_START and TRX_END Interrupts in Basic Operating Mode (see register 0x0F – IRQ_STATUS)

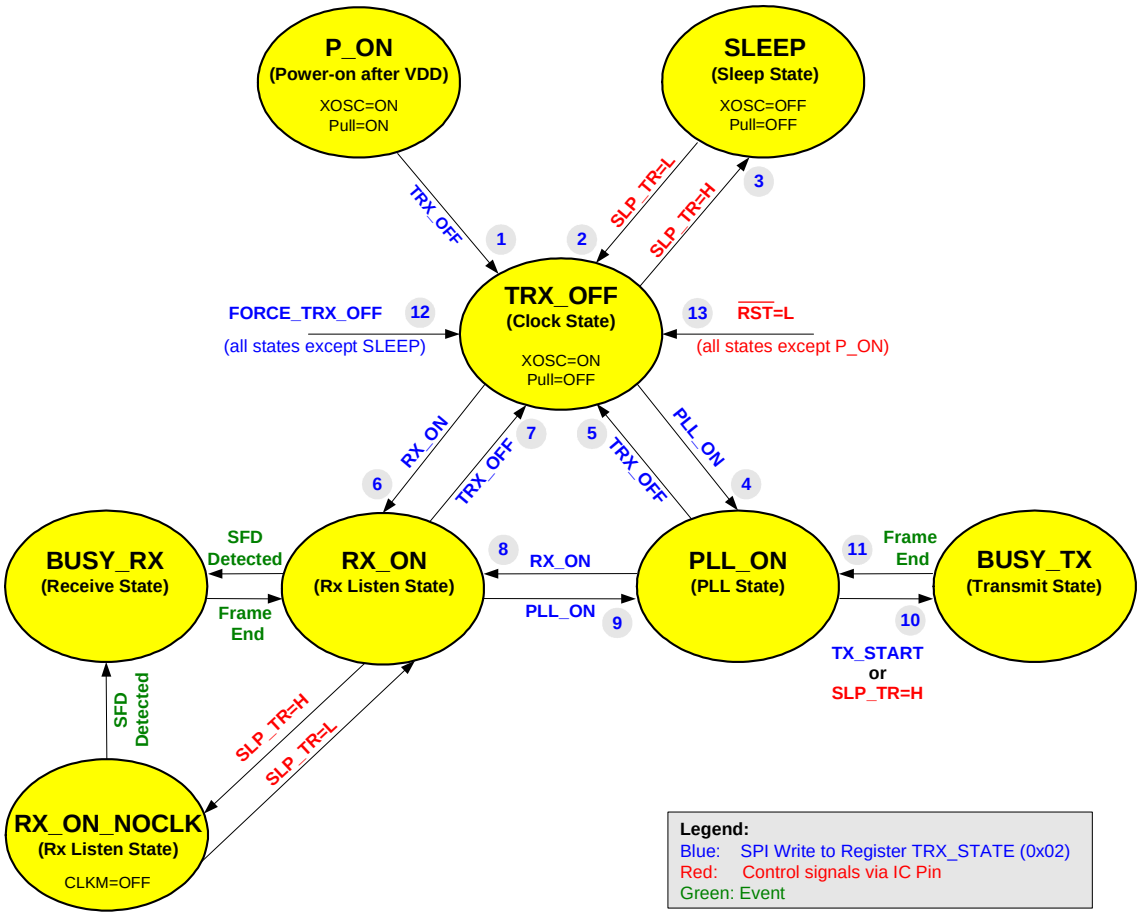


7 Operating Modes

7.1 Basic Operating Mode

This section summarizes all states to provide the basic functionality of the AT86RF230, such as receiving and transmitting frames, and powering up and down. The Basic Operating Mode is designed for IEEE 802.15.4-2003 applications; the corresponding radio transceiver states are shown in **Figure 7-1**.

Figure 7-1. Basic Operating Mode State Diagram (for State Transition Timing Data Refer to Table 7-3)



7.1.1 State Control

The radio transceiver state is controlled by two signal pins (SLP_TR, $\overline{\text{RST}}$) and the register 0x02 (TRX_STATE). A successful state change can be confirmed by reading the radio transceiver status from register 0x01 (TRX_STATUS).

The pin SLP_TR is a multifunctional pin. Depending on the radio transceiver state rising edge of SLP_TR causes the following state transitions:

- TRX_OFF → SLEEP
- RX_ON → RX_ON_NOCLK
- PLL_ON → BUSY_TX

The pin $\overline{\text{RST}}$ causes a reset of all registers and forces the radio transceiver into TRX_OFF state. Except, if the device is in the P_ON state it remains in the P_ON state.

For all states, the state change commands FORCE_TRX_OFF or TRX_OFF lead to a transition into TRX_OFF state. If the radio transceiver is in the BUSY_RX or BUSY_TX state, the command FORCE_TRX_OFF interrupts the active receiving or transmitting process, and forces an immediate transition. A TRX_OFF command is stored until a frame currently being received or transmitted is finished. After the end of the frame, the transition to TRX_OFF is performed.

Register Description

Table 7-1. TRX_STATUS (0x01) – Status of Basic Operating Mode

Bit	Field Name	Reset	R/W	Comments
7	CCA_DONE	0	R	0: CCA calculation in progress 1: CCA calculation done
6	CCA_STATUS	0	R	Indicates an idle channel from CCA module. 0: channel is busy 1: channel is idle
5		0	R	Reserved
4:0	TRX_STATUS	0	R	Current radio transceiver status. 0: P_ON 1: BUSY_RX 2: BUSY_TX 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 15: SLEEP 17: BUSY_RX_AACK 18: BUSY_TX_ARET 22: RX_AACK_ON 25: TX_ARET_ON 28: RX_ON_NOCLK 29: RX_AACK_ON_NOCLK 30: BUSY_RX_AACK_NOCLK 31: STATE_TRANSITION_IN_PROGRESS

Table 7-2. TRX_STATE (0x02) - Control of Basic Operating Mode

Bit	Field Name	Reset	R/W	Comments
7:5	TRAC_STATUS	0	R	0: SUCCESS 3: CHANNEL_ACCESS_FAILURE 5: NO_ACK All other values are reserved.
4:0	TRX_CMD	0	R/W	Radio transceiver control commands: 0: NOP 2: TX_START 3: FORCE_TRX_OFF 6: RX_ON 8: TRX_OFF (Clock Mode) 9: PLL_ON (TX_ON) 22: RX_AACK_ON 25: TX_ARET_ON All other values are mapped to NOP.

7.1.2 Basic Operating Mode Description

7.1.2.1 P_ON - Power-on after V_{DD}

When the external supply voltage (V_{DD}) is first supplied to the radio transceiver, the system is in the P_ON state. An on-chip reset is performed. The crystal oscillator gets activated and the master clock is provided to the CLKM pin after the crystal oscillator has stabilized. CLKM can be used as a clock source to the microcontroller.

The on-chip power-on-reset sets all registers to their default values. A dedicated reset signal from the microcontroller at the pin $\overline{RST}$ is not necessary, but recommended for hardware / software synchronization reasons. The reset impulse should have a minimum length as specified in section 9.4.

All digital inputs have pull-up or pull-down resistors (see Table 4-4). This is necessary to support microcontrollers where GPIO signals are floating after reset. The input pull-up and pull-down resistors are disabled when the radio transceiver leaves the P_ON state.

Prior to leaving P_ON, the microcontroller must set the pins to the default operating values: SLP_TR = L and $\overline{RST}$ = H.

Once the supply voltage has stabilized and the crystal oscillator has settled (see section 9.5, parameter “Reference oscillator settling time”), a valid SPI write access to the register TRX_STATE with the values TRX_OFF or FORCE_TRX_OFF takes the radio transceiver out of the P_ON state.

7.1.2.2 SLEEP – Sleep State

In SLEEP state, the entire radio transceiver is disabled. No circuitry is operating. If CLKM is enabled, the SLEEP state is entered 35 CLKM cycles after the rising edge at SLP_TR. At that time CLKM is turned off. The current consumption is reduced to leakage current only. This state can only be entered from state TRX_OFF, by setting the pin SLP_TR = H.

Setting SLP_TR = L returns the radio transceiver to the TRX_OFF state. The register contents remain valid while the content of the Frame Buffer is lost.

7.1.2.3 TRX_OFF – Clock State

In TRX_OFF state the SPI interface and the crystal oscillator are enabled. The digital voltage regulator (DVREG) is enabled and provides 1.8V to the digital core to make the Frame Buffer

available (see section 8.3). The microcontroller can access all digital functions and if enabled, the CLKM output supplies a clock. The pins SLP_TR and $\overline{\text{RST}}$ are enabled for state control.

7.1.2.4 PLL_ON – PLL State

Entering the PLL_ON state from TRX_OFF state enables the analog voltage regulator (AVREG) first. After the voltage regulator has been settled, the PLL frequency synthesizer is enabled. When the PLL has been settled at the receive frequency, a successful PLL lock is indicated by issuing a PLL_LOCK interrupt.

If an RX_ON command is issued in PLL_ON state, the receiver is immediately enabled. If the PLL has not been settled before, actual frame reception can only happen once the PLL has locked.

The PLL_ON state corresponds to the TX_ON state in IEEE 802.15.4-2003.

7.1.2.5 RX_ON and BUSY_RX – RX Listen and Receive State

In RX_ON state the digital receiver blocks and the PLL frequency synthesizer are enabled. The transition from TRX_OFF state to RX_ON state is started by writing the RX_ON command to register 0x02 (TRX_STATE).

The receive mode is internally divided into RX_ON state and BUSY_RX state. There is no difference between these states with respect to the analog radio transceiver circuitry. During RX_ON state, only the preamble detection of the digital signal processing is running. When a preamble and a valid SFD are detected, the digital receiver is turned on, and the radio transceiver enters the BUSY_RX state.

7.1.2.6 RX_ON_NOCLK – RX Listen State without CLKM

If the radio transceiver is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 6) is supported by the AT86RF230 using the state RX_ON_NOCLK.

This state can only be entered by setting SLP_TR = H while the AT86RF230 is in the RX_ON state. The CLKM pin is disabled 35 clock cycles after the rising edge at the SLP_TR pin. This allows the microcontroller to complete its power-down sequence. The reception of a frame is indicated to the microcontroller by a RX_START interrupt. CLKM is turned on again, and the radio transceiver enters the BUSY_RX state (see section 6.3 and **Figure 6-14**).

The end of the transaction is indicated to the microcontroller by a TRX_END interrupt. After the transaction has been completed, the radio transceiver enters the RX_ON state. The radio transceiver only reenters the RX_ON_NOCLK state, when the next rising edge of SLP_TR pin occurs.

If the radio transceiver is in the RX_ON_NOCLK state, and the SLP_TR pin is reset to logic low, it enters the RX_ON state, and it starts to supply clock on the CLKM pin again.

In states RX_ON_NOCLK and RX_ON, the current consumption is about the same, because only the CLKM output is switched off in state RX_ON_NOCLK.

7.1.2.7 BUSY_TX – Transmit State

A transmission can only be started at state PLL_ON. There are two ways to start a transmission:

- Rising edge of SLP_TR
- TX_START command to register 0x02 (TRX_STATE).

Either of these causes the AT86RF230 to enter the BUSY_TX state.

During the transition to BUSY_TX state, the PLL frequency shifts to the transmit frequency. Transmission of the first data chip of the preamble starts after 16 µs to allow PLL settling and PA ramping, see **Figure 6-15**.

When the frame transmission is completed, the radio transceiver automatically turns off the power amplifier and returns to PLL_ON state.

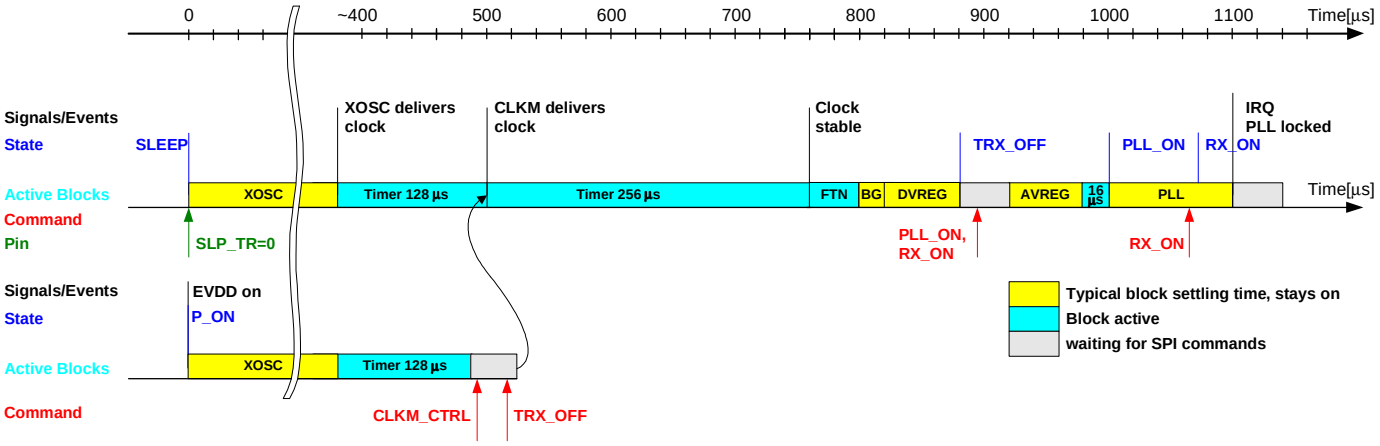
7.1.3 Basic Mode Timing

The following paragraphs depict the transitions between states and their timing.

7.1.3.1 Wake-up Procedure

The power-on sequence and the wake-up procedure is shown in **Figure 7-2**.

Figure 7-2. Wake-Up Procedure from SLEEP and P_ON to RX_ON (PLL Locked)



Setting pin SLP_TR = L in SLEEP state enables the crystal oscillator. After 0.4 ms (typ.), the internal clock signal is available. After another 128 µs the clock signal is provided at the CLKM pin if enabled. An additional 256 µs timer ensures that frequency stability is sufficient to drive filter tuning (FTN) and the PLL. After the digital voltage regulator has been settled, the radio transceiver enters the TRX_OFF state and waits for further commands.

In TRX_OFF state, entering the commands PLL_ON state or RX_ON initiates a ramp-up sequence of the analog voltage regulator. RX_ON state can be entered any time during PLL_ON state regardless whether the PLL has already locked.

When the wake-up sequence is started from P_ON state (V_{DD} first applied to the radio transceiver) the state machine stops after the 128 µs timer expires to wait for a valid TRX_OFF command from the microcontroller. The default CLKM frequency in P_ON state is 1 MHz.

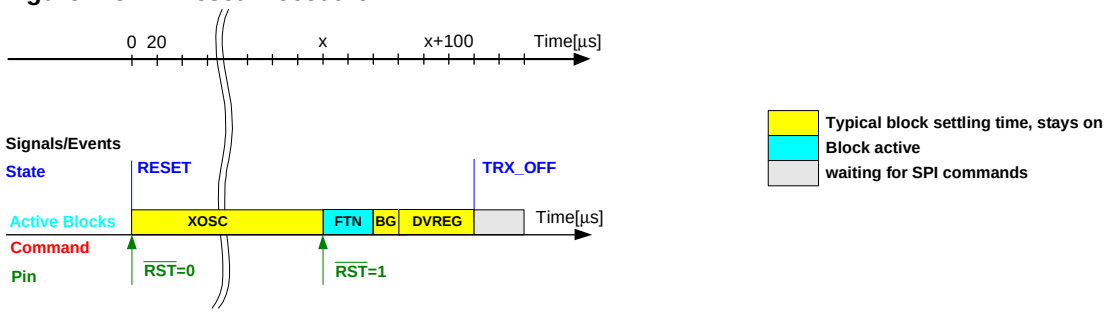
7.1.3.2 Reset Procedure

$\overline{\text{RST}}$ = L sets all registers to their default values. After releasing the reset pin ($\overline{\text{RST}}$ = H) a calibration cycle of the FTN is started and the digital voltage regulator is turned on. The state TRX_OFF is entered and the status of the main state machine changes from STATE_TRANSITION_IN_PROGRESS to TRX_OFF.

This sequence is identical for all radio transceiver states except in state P_ON. The state machine does not leave the state P_ON after a reset in this state. Instead, the procedure described in section 7.1.2.1 must be followed in order to enter the TRX_OFF state for the very first time. **Figure 7-3** describes the reset procedure once the P_ON state was left.

Note that the access to the device should not occur earlier than 625 ns after releasing the reset pin.

Figure 7-3. Reset Procedure



7.1.3.3 State Transition Timing

The transition numbers correspond to **Figure 7-1**. See the measurement setup in **Figure 5-1**.

Table 7-3. State Transition Timing

No	Symbol	Transition	Time [µs] (typical)	Comments
1	t_{TR1}	P_ON → TRX_OFF	880	Depends on external bypass capacitor at DVDD (1 µF nom) and crystal oscillator setup (C_L = 10 pF)
2	t_{TR2}	SLEEP → TRX_OFF	880	Depends on external bypass capacitor at DVDD (1 µF nom) and crystal oscillator setup (C_L = 10 pF)
3	t_{TR3}	TRX_OFF → SLEEP	35	f_{CLKM} = 1 MHz
4	t_{TR4}	TRX_OFF → PLL_ON	180	Depends on external bypass capacitor at AVDD (1 µF nom).
5	t_{TR5}	PLL_ON → TRX_OFF	1	
6	t_{TR6}	TRX_OFF → RX_ON	180	Depends on external bypass capacitor at AVDD (1 µF nom).
7	t_{TR7}	RX_ON → TRX_OFF	1	
8	t_{TR8}	PLL_ON → RX_ON	1	
9	t_{TR9}	RX_ON → PLL_ON	1	
10	t_{TR10}	PLL_ON → BUSY_TX	16	When asserting SLP_TR pin first symbol transmission is delayed by 16 µs (PLL settling and PA ramp up).
11	t_{TR11}	BUSY_TX → PLL_ON	32	32 µs PLL settling time to TX frequency
12	t_{TR12}	All states → TRX_OFF	1	Using TRX_CMD FORCE_TRX_OFF (see register 0x02), not valid for SLEEP mode
13	t_{TR13}	$\overline{RST}$ = L → TRX_OFF	120	Depends on external bypass capacitor at DVDD (1 µF nom), not valid for P_ON mode

The state transition timing is calculated based on the timing of the individual blocks shown in **Figure 7-2**. The worst case values include maximum operating temperature, minimum supply voltage, and device parameter variations.

Table 7-4. Block Settling Time

Block	Time [µs] (typical)	Time [µs] (worst case)	Comments
XOSC	500	1000	Until clock signal is provided at CLKM pin. Depends on crystal Q factor and load capacitor
DVREG	60	1000	Depends on external bypass capacitor at DVDD (CB3 = 1 µF nom., 10 µF worst case)
AVREG	60	1000	Depends on external bypass capacitor at AVDD (CB1 = 1 µF nom., 10 µF worst case)
PLL, initial	100	150	
PLL, RX → TX	16		PLL settling time
PLL, TX → RX	32		PLL settling time

7.2 Extended Operating Mode

The Extended Operating Mode goes beyond the basic radio transceiver functionality provided by the Basic Operating Mode to support specific functionality requested by the IEEE 802.15.4-2003 standard such as automatic acknowledgement and automatic frame retransmission. This releases the software developer from the implementation of this functionality using the Basic Operation Mode. This results in a more efficient IEEE 802.15.4-2003 software MAC implementation including reduced code size, the possible use of a smaller microcontroller or the ability to simplify the handling of time-critical tasks.

The Extended Operating Mode is designed to support IEEE 802.15.4-2003 standard compliant frames. While using the Extended Operating Mode for direct data transmissions, the AT86RF230 radio transceiver supports:

- Automatic address filtering
- Automatic acknowledgement (RX_AACK) and
- Automatic CSMA-CA with optional frame retransmission (TX_ARET)

The Extended Operating Mode does not support slotted CSMA-CA and indirect data transmissions.

The TX_ARET transaction consists of:

- CSMA-CA including automatic retry
- Frame transmission and automatic FCS field generation
- Reception of ACK frame (if ACK was requested)
- Automatic retry of transmissions if ACK was expected but not received
- Interrupt signaling with return code

The RX_AACK transaction consists of:

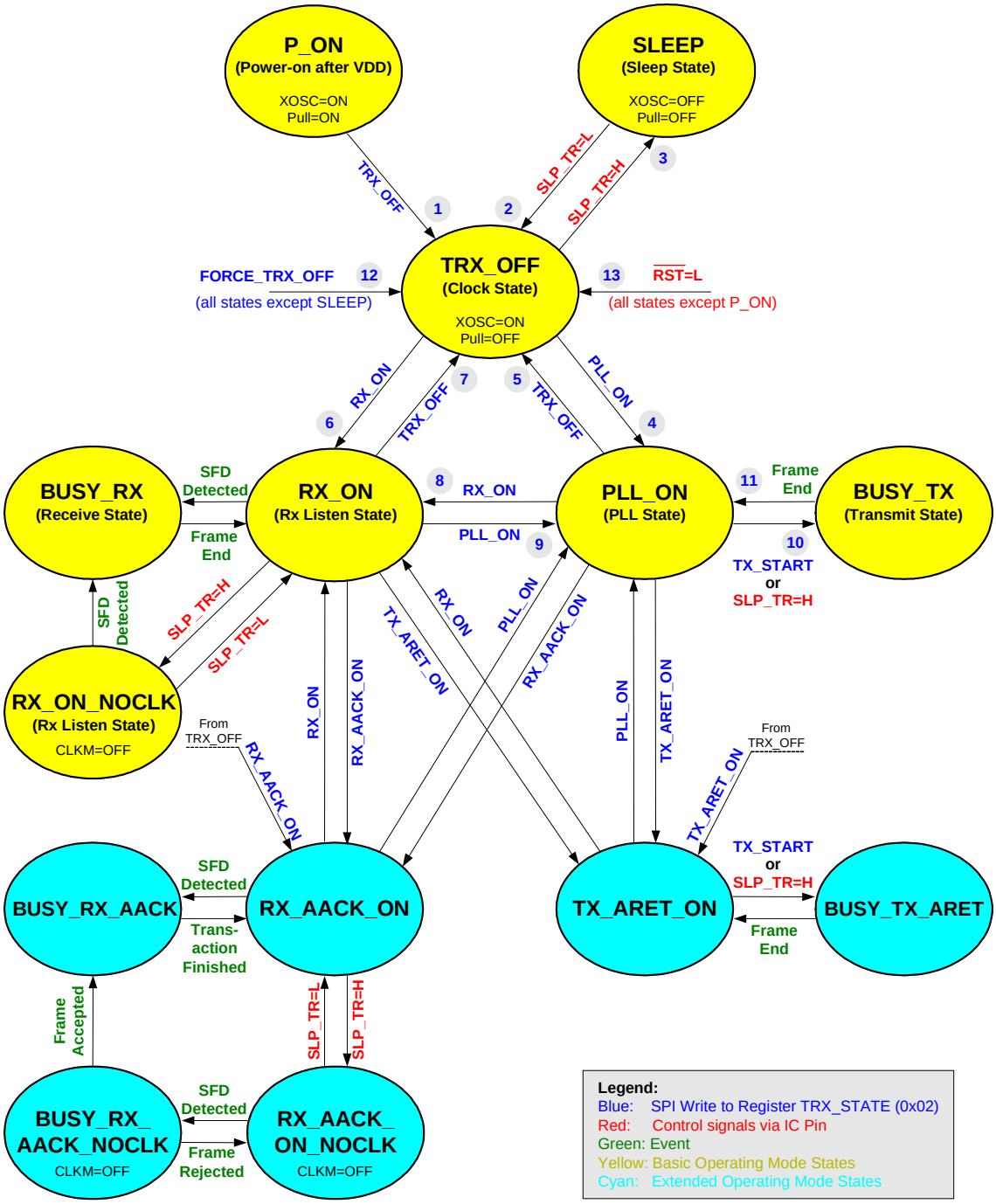
- Frame reception and automatic FCS check
- Address filtering
- Interrupt indicating frame reception, if it passes address filtering and FCS check
- Automatic ACK frame transmission (if the received frame passed the address filter and FCS check and if an ACK is required by the frame type and ACK request)

Automatic FCS generation can be used in conjunction with the TX_ARET states. In RX_AACK states, an automatic FCS check is always performed for incoming frames. To generate a valid ACK frame the automatic FCS generation must be enabled in RX_AACK states.

In RX_AACK states, an ACK frame is always sent with the frame pending subfield set to 0. In TX_ARET states, an ACK is accepted if the FCS is valid, and if the sequence number of the ACK matches the sequence number of the previously transmitted frame. The value of the frame pending subfield is ignored.

A state diagram of the Extended Operating Mode states is shown in **Figure 7-4**. Yellow marked states represent the Basic Operating Mode, blue marked states represent the Extended Operating Mode.

Figure 7-4. Extended Operating Mode State Diagram



7.2.1 Configuration and State Control

The use of the Extended Operating Mode is based on Basic Operating Mode functionality, for details see section 7.1.

Configuration

RX_AACK:

- Set register bit TX_AUTO_CRC_ON = 1 (register 0x05)
- Setup registers 0x20 – 0x2B for PAN-ID and IEEE address
- Configure register bit I_AM_COORD (register 0x2E)

TX_ARET:

- Set register bit TX_AUTO_CRC_ON = 1 (register 0x05)
- Configure CSMA-CA
  - MAX_FRAME_RETRIES (register 0x2C)
  - MAX_CSMA_RETRIES (register 0x2C)
  - CSMA_SEED (registers 0x2D, 0x2E)
  - MIN_BE (register 0x2E)
- Configure CCA (see section 8.7)

The MIN_BE register bits (register 0x2E) sets the minimum back-off exponent (refer to the IEEE 802.15.4-2003 standard), and the CSMA_SEED_0 and CSMA_SEED_1 register bits (registers 0x2D, 0x2E) define a random seed for the back-off-time random-number generator in the AT86RF230. The register bits MAX_CSMA_RETRIES (register 0x2C) configures how often the radio transceiver retries the CSMA-CA algorithm after a busy channel is detected. MAX_FRAME_RETRIES (register 0x2C) defines the maximum number of frame retransmissions.

State Control

RX_AACK:

The state RX_AACK_ON is entered by writing the command RX_AACK_ON to the register bits TRX_CMD in register 0x02 (TRX_STATE). The state change can be confirmed by reading register 0x01 (TRX_STATUS), that changes to RX_AACK_ON or BUSY_RX_AACK on success.

TX_ARET:

Similarly, TX_ARET_ON state is activated by setting register bits TRX_CMD (register 0x02) to TX_ARET_ON. The radio transceiver is in the TX_ARET_ON state after TRX_STATUS (register 0x01) changes to TX_ARET_ON.

Register Summary

Table 7-5. Register Summary

Reg.-Addr.	Register Name	Description
0x01	TRX_STATUS	Radio transceiver status, CCA result
0x02	TRX_STATE	State control
0x05	PHY_TX_PWR	TX_AUTO_CRC_ON
0x20 - 0x2B		Address filter configuration
0x2C	XAH_CTRL	Retries value control
0x2D	CSMA_SEED_0	CSMA seed value
0x2E	CSMA_SEED_1	CSMA seed value, I_AM_COORD, MIN_BE

Register Description

Table 7-6. TRX_STATUS (0x01) - Status of Extended Operating Mode

Bit	Field Name	Reset	R/W	Comments
7	CCA_DONE	0	R	0: CCA calculation in progress 1: CCA calculation done
6	CCA_STATUS	0	R	Indicates an idle channel from CCA module. 0: channel is busy 1: channel is idle
5		0	R	Reserved
4:0	TRX_STATUS	0	R	Current radio transceiver status. 0: P_ON 1: BUSY_RX 2: BUSY_TX 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 15: SLEEP 17: BUSY_RX_AACK 18: BUSY_TX_ARET 22: RX_AACK_ON 25: TX_ARET_ON 28: RX_ON_NOCLK 29: RX_AACK_ON_NOCLK 30: BUSY_RX_AACK_NOCLK 31: STATE_TRANSITION_IN_PROGRESS

Table 7-7. TRX_STATE (0x02) – Control of Extended Operating Mode

Bit	Field Name	Reset	R/W	Comments
7:5	TRAC_STATUS	0	R	0: SUCCESS 3: CHANNEL_ACCESS_FAILURE 5: NO_ACK All other values are reserved.
4:0	TRX_CMD	0	R/W	Radio transceiver control commands: 0: NOP 2: TX_START 3: FORCE_TRX_OFF 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 22: RX_AACK_ON 25: TX_ARET_ON All other values are mapped to NOP.

7.2.2 Interrupt Handling in Extended Operating Mode

The interrupts in the Extended Operating Mode are handled differently compared to the Basic Operating Mode (see section 6.4). The number of possible interrupts is reduced to a necessary minimum of events. This minimizes the interaction between microcontroller and AT86RF230 to reduce the overall power consumption. The differences in the interrupt handling are described in the following table.

Table 7-8. Interrupt Description for Extended Operating Mode

IRQ Register Bit	IRQ Name	Special handling in Extended Operating Mode
7	IRQ_7: BAT_LOW	No special handling
6	IRQ_6: TRX_UR	No special handling
3	IRQ_3: TRX_END	TX_ARET: Indicates the completion of TX_ARET algorithm. RX_AACK: Indicates the successful frame reception. Frame data can be uploaded to the microcontroller.
2	IRQ_2: RX_START	Not used
1	IRQ_1: PLL_UNLOCK	Disabled for regular operation. In case of occurrence, the device status needs to be examined (see AVR2001 "AT86RF230 - Software Programmer's Guide").
0	IRQ_0: PLL_LOCK	Disabled for regular operation. In case of occurrence, the device status needs to be examined (see AVR2001 "AT86RF230 - Software Programmer's Guide").

7.2.3 Extended Operation Mode Description

7.2.3.1 RX_AACK_ON – Receive with Automatic ACK

In the RX_AACK_ON state, the radio transceiver listens for incoming frames. After detecting a frame start, the radio transceiver parses the frame contents of the MAC header (MHR). The filtering procedure as described in IEEE 802.15.4-2003 chapter 7.5.6.2. (third level filter rules) is applied to the frame. It accepts only frames that satisfy all of the following requirements (quote from IEEE 802.15.4-2003):

- The frame type subfield of the frame control field shall not contain an illegal frame type.
- If the frame type indicates that the frame is a beacon frame, the source PAN identifier shall match macPANId unless macPANId is equal to 0xFFFF, in which case the beacon frame shall be accepted regardless of the source PAN identifier.
- If a destination PAN identifier is included in the frame, it shall match macPANId or shall be the broadcast PAN identifier (0xFFFF).
- If a short destination address is included in the frame, it shall match either macShortAddress or the broadcast address (0xFFFF). Otherwise, if an extended destination address is included in the frame, it shall match an ExtendedAddress.
- If only source addressing fields are included in a data or MAC command frame, the frame shall be accepted only if the device is a PAN coordinator and the source PAN identifier matches macPANId. Any frames rejected by these rules are discarded.

A frame is also discarded if the FCS is invalid. Otherwise, the TRX_END interrupt is issued after the reception of the frame is completed. The microcontroller can then upload the frame.

The AT86RF230 detects whether an ACK frame needs to be sent. In that case, the radio transceiver automatically generates an ACK frame and transmits this frame 12 symbol periods after the end of the received frame. The frame pending subfield is always 0. The sequence number is copied from the received frame. During these operations the radio transceiver remains in BUSY_RX_AACK state.

The general functionality of the RX_AACK is shown in **Figure 7-5**.

The timing of an RX_AACK transaction is shown in **Figure 7-6**. An example data frame of length 10 with an ACK request is received. A state change to BUSY_RX_AACK is performed after SFD detection. The completion of the frame reception is indicated by a TRX_END interrupt. The ACK frame is transmitted after a wait period of 12 symbols (192 µs).

Figure 7-5. Flow Diagram of RX_AACK

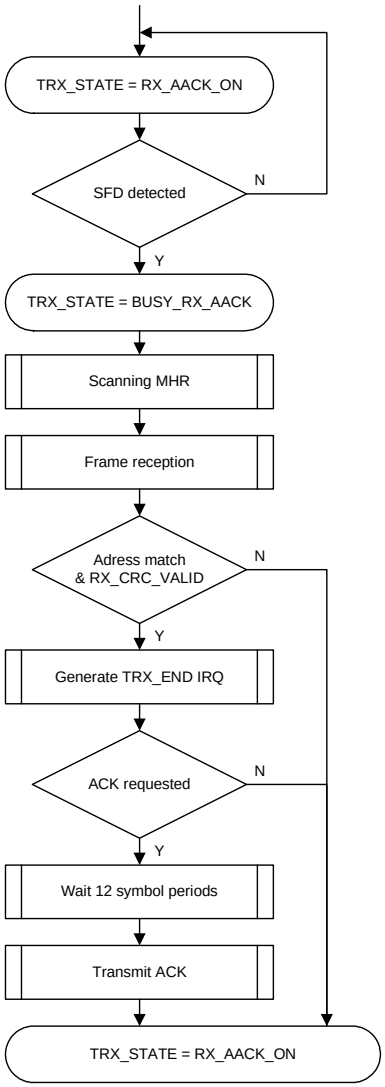
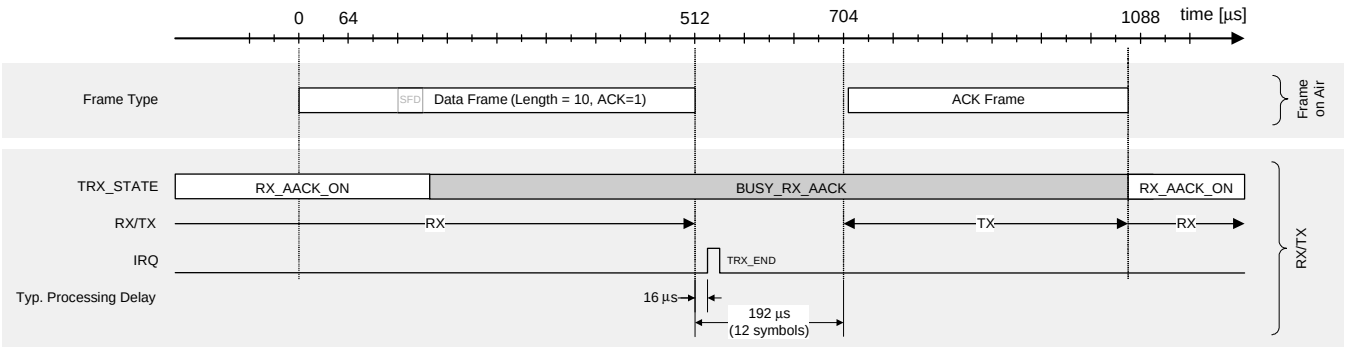


Figure 7-6. Example Timing of an RX_AACK Transaction



7.2.3.2 TX_ARET_ON – Transmit with Automatic CSMA-CA Retry

The implemented TX_ARET algorithm is shown in **Figure 7-7**.

In TX_ARET states, the AT86RF230 first executes the CSMA-CA algorithm. If the channel is idle, the previously downloaded frame is transmitted. If the acknowledgement request subfield is 1 in a MAC command or data frame, the radio transceiver checks for an ACK reply. It indicates the completion of the transaction by issuing a TRX_END interrupt. After the TRX_END interrupt, the microcontroller may read the value of the TRAC_STATUS register bits (register 0x02) to determine whether or not the transaction was successful.

The TX_ARET transaction is started by either a rising edge on SLP_TR pin or writing a TX_START command to register 0x02 (TRX_STATE), see **Figure 7-8**. The radio transceiver executes the CSMA-CA algorithm as defined by IEEE 802.15.4-2003 section 7.5.1.4. If a clear channel is detected during CSMA-CA execution, the radio transceiver proceeds to transmit the frame.

It is recommended to download the transmit data before starting the transaction.

During transmission the AT86RF230 parses the frame control field of the downloaded frame to check if an ACK reply is expected.

If an ACK is expected, the radio transceiver switches into receive mode to wait for a valid ACK reply. If no valid ACK is received or a timeout (after 544 µs) occurred, the radio transceiver retries the entire transaction, including CSMA-CA execution. This repeats until the frame has been acknowledged or the maximum number of retransmissions (as set by the register bits MAX_FRAME_RETRIES in register 0x2C) has been reached. In this case, the TRX_END interrupt is issued and the value of TRAC_STATUS is set to NO_ACK. If a valid ACK is found, the TRX_END interrupt is issued. In this case, TRAC_STATUS is set to SUCCESS.

If no ACK is expected, the radio transceiver issues a TRX_END interrupt after the frame transmission has been completed. The value of register bits TRAC_STATUS (register 0x02) is set to SUCCESS.

If the CSMA-CA did not detect a clear channel, the channel access is retried as specified by the register bits MAX_CSMA_RETRIES (register 0x2C). In case that CSMA-CA does not detect a clear channel after MAX_CSMA_RETRIES, it aborts the transaction, issues the TRX_END interrupt, and sets the value of the TRAC_STATUS register bits to CHANNEL_ACCESS_FAILURE.

Figure 7-7. Flow Diagram of TX_ARET

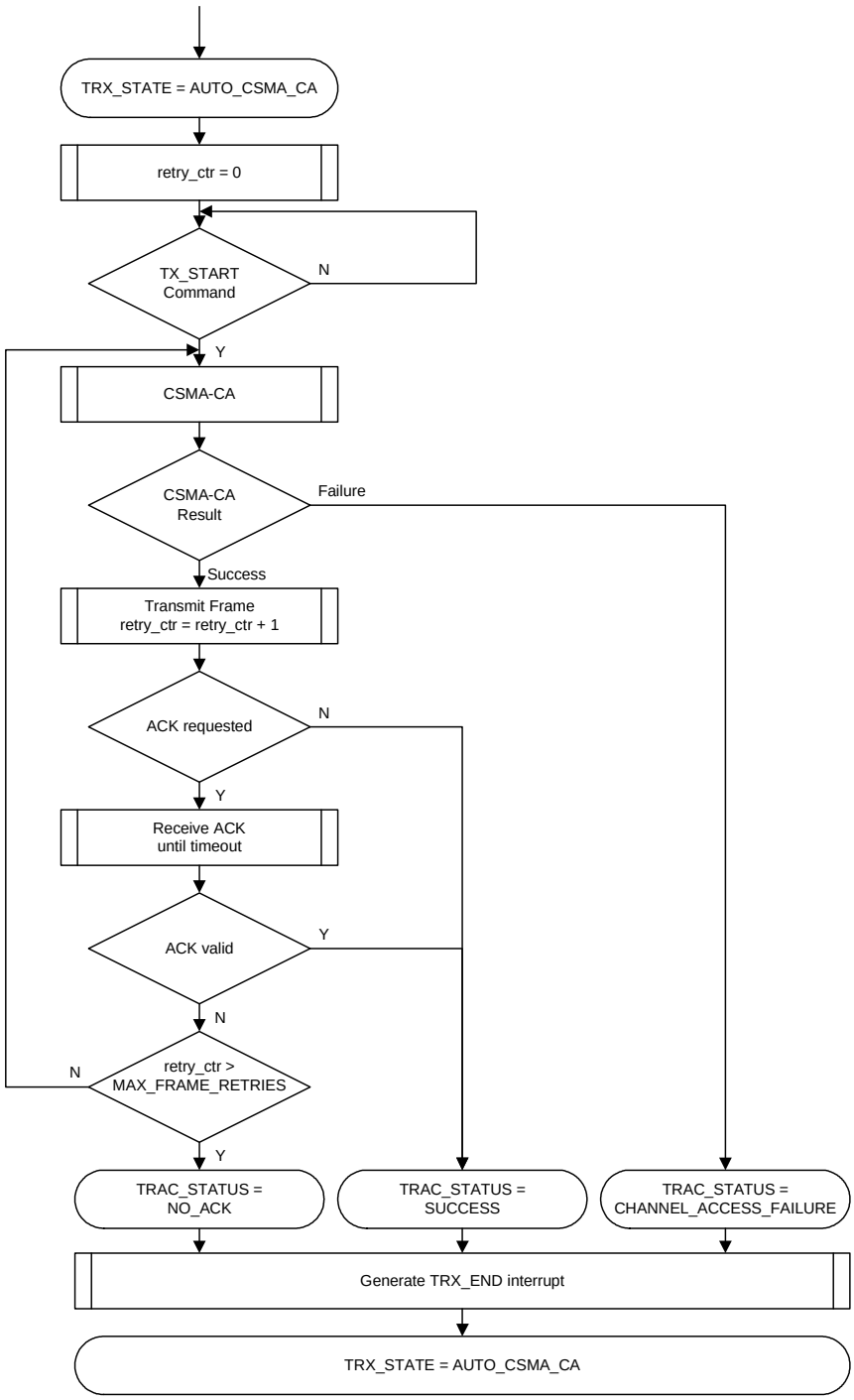
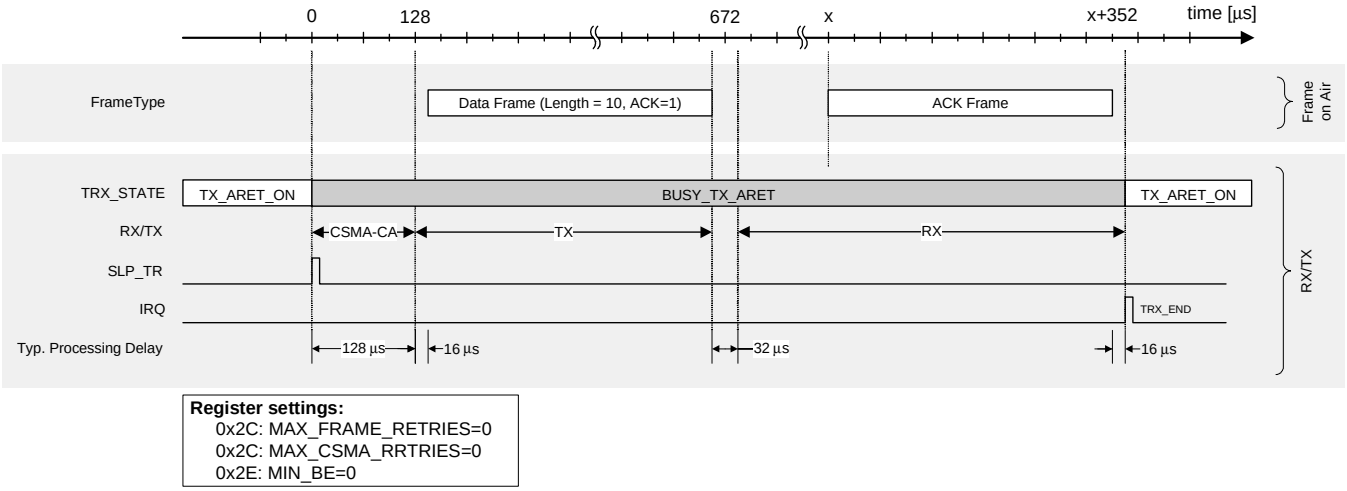


Figure 7-8. Timing Example of a TX_ARET Transaction



7.2.3.3 RX_AACK_NOCLK – RX_AACK_ON without CLKMf

If the AT86RF230 is listening for an incoming frame and the microcontroller is not running an application, the microcontroller can be powered down to decrease the total system power consumption. This special power-down scenario for systems running in clock synchronous mode (see section 6) is supported by the AT86RF230 using the state RX_AACK_ON_NOCLK.

This RX_AACK_NOCLK state is entered by setting SLP_TR = H while the AT86RF230 is in the RX_AACK_ON state. The CLKM pin is disabled 35 clock cycles after the rising edge at the SLP_TR pin. This allows the microcontroller to complete its power-down sequence.

In case of the reception of a valid frame, the TRX_END interrupted is issued and CLKM is turned on again. A received frame is considered valid if it passes address filtering and has a correct FCS. If an ACK was requested the radio transceiver enters BUSY_RX_AACK state and follows the procedure described in section 7.2.3.1.

After the transaction has been completed, the radio transceiver reenters the RX_AACK_ON state.

The radio transceiver reenters the RX_AACK_ON_NOCLK state only, when the next rising edge at SLP_TR pin occurs.

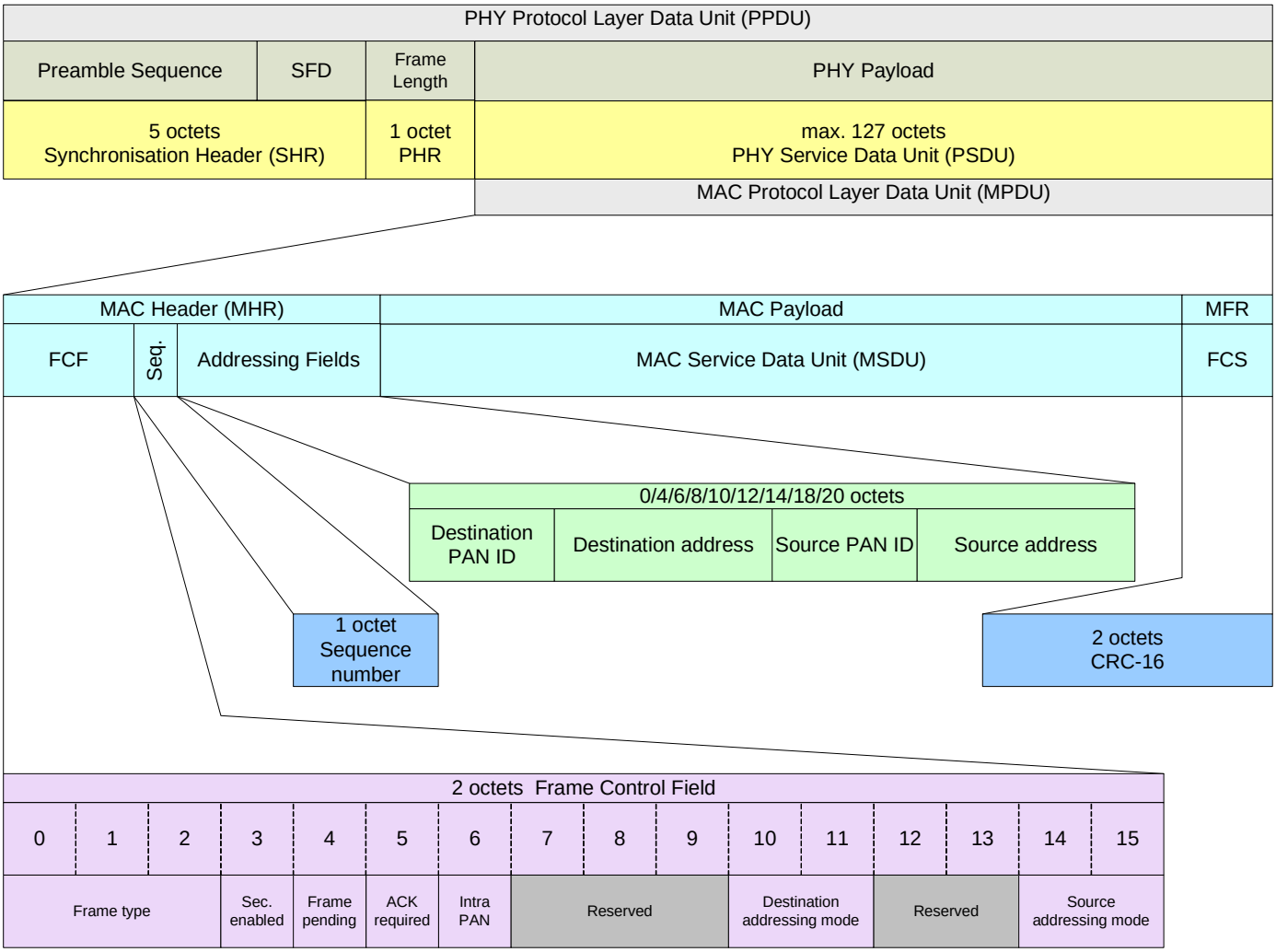
If the radio transceiver is in the RX_AACK_ON_NOCLK state, and the SLP_TR pin is reset to logic low, it enters the RX_AACK_ON state, and it starts to supply clock on the CLKM pin again.

8 Functional Description

8.1 Introduction - Frame Format

Figure 8-1 provides an overview of the overall frame structure defined by the IEEE 802.15.4-2003 standard.

Figure 8-1. IEEE 802.15.4-2003 Frame Format (Upper Part: PHY-Layer Frame Structure; Bottom Part: MAC-Layer Frame Elements Details)



8.1.1 PHY Protocol Layer Data Unit (PPDU)

8.1.1.1 Synchronization Header (SHR)

The SHR consists of a four-octet preamble field (all zero), followed by a single SFD which has the predefined value 0xA7. When transmitting, the SHR is automatically generated by the AT86RF230, and prefixed to the frame that has been downloaded by the microcontroller. The transmission of the SHR requires 160 µs (10 symbols). This allows the microcontroller to

initiate a transmission without having the current frame data already loaded into the radio transceiver, and subsequently start downloading the frame contents afterwards.

During frame reception, the SHR is matched by the receiver logic, and used to determine the time where the incoming frame actually starts.

8.1.1.2 PHY Header (PHR)

The PHY header consists of a single octet following the SHR. The least significant 7 bits of that octet denote the frame length of the following PSDU, while the most significant bit of that octet is reserved, and must be written as 0.

The PHR is to be supplied by the microcontroller during frame download.

During reception, the frame length is passed up during frame upload as the first octet, with the most significant bit always set to 0.

8.1.1.3 PHY Payload (PHY Service Data Unit, PSDU)

The PSDU has a variable length between one and 127 octets.

8.1.2 MAC Protocol Layer Data Unit (MPDU)

8.1.2.1 MAC Header (MHR) Fields

The MAC header consists of the Frame Control Field (FCF), a sequence number, and the addressing fields (which are of variable length, and can even be empty in certain situations).

8.1.2.2 Frame Control Field (FCF

The FCF consists of 16 bits, and occupies the first two octets of the MPDU.

Bit [2:0]: describe the frame type. Table 8-1 summarizes frame types defined by IEEE 802.15.4-2003.

Table 8-1. IEEE 802.15.4-2003 Frame Types

Bits[2:0]	Description
000	Beacon frame
001	Data frame
010	Acknowledgment (ACK) frame
011	MAC command frame

Values other than those mentioned in Table 8-1 are reserved, and should not be used.

Bit 3: indicates whether security processing applies to this frame. This field is not used by the AT86RF230.

Bit 4: is the “frame pending” subfield. This field can be set in an acknowledgment frame to indicate to the node receiving the acknowledgment frame that the node sent the acknowledgment frame has more data to send.

Bit 5: forms the “acknowledgment request” subfield. If this bit is set within a data or MAC command frame that is not broadcast, the recipient shall acknowledge the reception of the frame within the time specified by IEEE 802.15.4-2003 (i.e. within 192 µs for nonbeacon-enabled networks).

Bit 6: the “Intra-PAN” subfield indicates that in a frame where both, the destination and source addresses are present, the PAN ID is omitted from the source address field. This bit is evaluated by the address filter logic of the AT86RF230.

Bit [11:10]: the “Destination address mode” subfield describes the format of the destination address of the frame. The values of the address modes are summarized in Table 8-2, according to IEEE 802.15.4-2003:

Table 8-2. IEEE 802.15.4-2003 Address Modes

Bits[11:10] Bits[15:14]	Description
00	Address not present
01	Reserved, must not be used
10	Address is 16-bit short
11	Address is 64-bit extended address

If the destination address mode is either 2 or 3 (i.e. if the destination address is present at all), it always consists of a 16-bit PAN ID first, followed by either the 16-bit or 64-bit address as described by the mode.

Bit [15:14]: form the “Source address mode” subfield, with similar meaning as “Destination address mode”.

The address field description bits of the FCF (Bits 6, 10, 11, 14, 15) affect the address filter logic of the AT86RF230 while operating in RX_AACK states.

8.1.2.3 Sequence number

The one-octet sequence number following the FCF identifies a particular frame, so that duplicated frame transmissions can be detected. While operating in RX_AACK states, the content of this field is copied into the acknowledgment frame.

8.1.2.4 Addressing fields

The addressing fields terminate the MHR. The destination address (if present) is always transmitted first, followed by the source address (if present). Each address consists of the PAN ID and a device address. If both addresses are present, and the “Intra PAN” subfield in the FCF is set to 1, the source PAN ID is omitted.

Note that in addition to these general rules, IEEE 802.15.4-2003 further restricts the valid address combinations for the individual possible MAC frame types. For example, the situation where both addresses are omitted (source addressing mode = 0 and destination addressing mode = 0) is only allowed for acknowledgment frames. The address filter in the AT86RF230 has been designed to apply to IEEE 802.15.4-2003 compliant frames only.

8.1.2.5 MAC Service Data Unit (MSDU

This is the actual MAC payload. It is usually structured according to the individual frame type descriptions in IEEE 802.15.4-2003.

8.1.2.6 MAC Footer (MFR) Fields

The MAC footer consists of a two-octet Frame Checksum (FCS), for details refer to section 8.2.

8.2 Frame Check Sequence (FCS)

By definition, the frame check sequence main features are:

- Indicates bit errors
- Contains a CRC of length 16 bit
- Uses International Telecommunication Union (ITU) CRC polynomial

8.2.1 Overview

The FCS is intended for use at the PHY level to detect corrupted frames. It is computed by applying an ITU CRC polynomial to all transmitted bytes following the length field (MHR and MSDU fields). The frame check sequence has a length of 16 bit and is located in the last two bytes of a frame.

By default, the generation of the FCS bytes and the FCS is not applied by the AT86RF230. For transmit, the AT86RF230 can be configured to autonomously compute the FCS.

The Extended Operating Mode of the AT86RF230 autonomously handles the check and the generation of the FCS bytes. The register bit TX_AUTO_CRC_ON in register 0x05 (PHY_TX_PWR) needs to be set to 1 to enable this feature.

8.2.2 CRC calculation

The CRC polynomial used in IEEE 802.15.4-2003 networks is defined by

$$G_{16}(x) = x^{16} + x^{12} + x^5 + 1 \quad .$$

The FCS shall be calculated for transmission using the following algorithm:

Let

$$M(x) = b_0 x^{k-1} + b_1 x^{k-2} + \ldots + b_{k-2} x + b_{k-1}$$

be the polynomial representing the sequence of bits for which the checksum is to be computed. Multiply M(x) by x^{16}, giving the polynomial

$$N(x) = M(x) \cdot x^{16}.$$

Divide $N(x)$ modulo 2 by the generator polynomial, $G_{16}(x)$, to obtain the remainder polynomial,

$$R\ (x) = r_0 x^{15} + r_1 x^{14} + \ldots + r_{14} x + r_{15}$$

The FCS field is given by the coefficients of the remainder polynomial, $R\ (x)$.

Example:

Considering a 5 octet ACK frame. The MHR field consists of

0100 0000 0000 0000 0101 0110.

The leftmost bit (b_0) is transmitted first in time. The FCS would be following

0010 0111 1001 1110.

The leftmost bit (r_0) is transmitted first in time.

8.2.3 Automatic FCS generation

An automatic FCS generation is enabled by setting register bit TX_AUTO_CRC_ON. This allows the AT86RF230 to compute the FCS autonomously. For a frame with a frame length field specified as N ($3 \leq N \leq 127$), the FCS is calculated on the first N-2 octets in the Frame Buffer, and the resulting FCS field is transmitted in place of the last two octets from the Frame Buffer.

Example:

A frame transmission of length five with TX_AUTO_CRC_ON set, is started with a frame download of five bytes (the last two bytes can be omitted). The first three bytes are used for FCS generation, the last two bytes are replaced by the FCS.

8.2.4 Automatic FCS check

The Extended Operating Mode has an automatic FCS check. To enable the feature the bit TX_AUTO_CRC_ON needs to be set.

By using RX_AACK states, the FCS of the incoming frame is automatically checked. If it is not valid, the RX_AACK procedure does not accept that frame and no TRX_END interrupt is generated.

By using TX_ARET states, the FCS of an ACK is automatically checked. If it is not correct, the ACK is not accepted.

Note, there is no automatic FCS check available using the RX states of Basic Operating Mode.

8.3 Frame Buffer

The AT86RF230 contains a 128 byte dual port SRAM. One port is connected to the SPI interface, the other to the internal TX/RX module port. For data communication both ports are independent and simultaneously accessible. Access conflicts are indicated by a TRX under run (TRX_UR) interrupt. The Frame Buffer is used for the TX and RX operation of the device and can keep one IEEE 802.15.4-2003 TX or one RX frame of maximum length at a time.

The Frame Buffer is physically located in the digital low voltage domain; therefore Frame Buffer access is only possible if the digital voltage regulator is turned on. This is valid in all device states except in SLEEP and P_ON.

8.3.1 Frame Buffer Data Management

Data in Frame Buffer (received data or data to be transmitted) remains valid as long as

- No new frame is written into the buffer over SPI
- No new frame is received (in any BUSY_RX state)
- No state change into SLEEP state is made

If the radio transceiver is in any RX state an incoming frame with valid SFD field overwrites the Frame Buffer content 32 µs after the RX_START interrupt occurs, even if the RX_START interrupt is disabled. In case the device has to remain in RX_ON state after a frame reception, the Frame Buffer content needs to be uploaded to the microcontroller as soon as possible. To avoid an unintended Frame Buffer overwrite a state change to PLL_ON immediately after the frame detection is recommended.

If a received frame upload is delayed and during the upload process a new frame is received, a TRX_UR interrupt occurs. Even so, the old frame data can be read, if the SPI data rate is higher than the effective over air data rate. A minimum SPI clock rate of 1 MHz is recommended in this special case. Finally it is required to check the uploaded frame data integrity by a FCS check using the microcontroller.

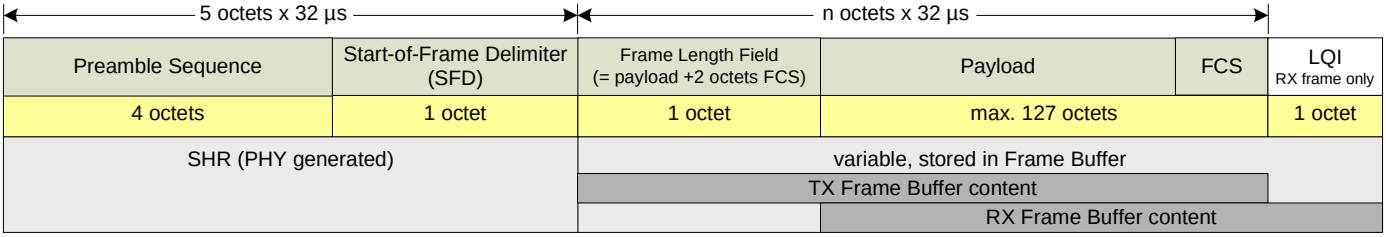
Using the Extended Operating Mode states TX_ARET_ON or TX_ARET_ON_NOCLK the radio transceiver switches to RX, if an acknowledgement was requested. In these states received frames are evaluated but not stored in the Frame Buffer. This allows the radio transceiver to wait for an acknowledgement frame and retry the data frame transmission without downloading them again.

A radio transceiver state change, except a transition to SLEEP, does not affect the Frame Buffer contents. If the radio transceiver is forced into SLEEP, the Frame Buffer is powered off and the stored data gets lost.

8.3.2 User accessible Frame Content

The AT86RF230 supports an IEEE 802.15.4-2003 compliant frame format as shown in **Figure 8-2**.

Figure 8-2. Frame Structure



A frame comprises two sections, the internally generated SHR field and the user accessible part stored in the Frame Buffer. The first part of the frame contains the preamble and the SFD field. The variable frame section contains the length field and the frame payload followed by the FCS field.

When using the Basic Operating Mode, the radio transceiver does only evaluate the Frame Length Field (PHR). In any of the receive states the PHY appends to an incoming frame the Link Quality Indicator (LQI) after the last received octet (e.g. FCS). The minimum frame length for a valid LQI value is two octets.

The Frame Buffer content differs depending on the direction of the communication (RX or TX). To access the data follow the procedures described in section 6.2.2.

In any of the receive states, the payload and the LQI value of a successfully received frame can be uploaded from the Frame Buffer. Using the Frame Buffer Access Mode the frame length information is added before the payload. If the SRAM Access Mode is used to read an RX frame, the frame length field cannot be accessed. The preamble or the SFD value cannot be read.

For data transmission it is recommended to download the frame content to the Frame Buffer before the transmission is started. The maximum frame size supported by the radio transceiver is 128 bytes, including PHR and FCS. The frame length must be calculated based on the payload and the two byte FCS. It must be stored as the first byte in the Frame Buffer followed by the payload and the FCS. If the TX_AUTO_CRC_ON bit is set in register 0x05 (PHY_TX_PWR), the FCS field is replaced by the automatically calculated FCS during frame transmission. The microcontroller needs to calculate the correct frame length including FCS field and can stop the SPI transfer right after the payload is stored into the Frame Buffer. There is no need to download dummy bytes when using automatic FCS generation.

For non IEEE 802.15.4-2003 frames, the minimum frame length supported by the device is one byte (Frame Length Field + 1 byte data).

8.4 Energy Detection (ED)

The main features for the Energy Detection module are:

- 85 unique energy levels defined
- 1 dB resolution
- ±5 dB accuracy

8.4.1 Overview

The receiver Energy Detection measurement is used by a network layer as part of a channel selection algorithm. It is an estimation of the received signal power within the bandwidth of an IEEE 802.15.4-2003 channel. No attempt is made to identify or decode signals on the channel. The ED value is calculated by averaging RSSI values over eight symbols.

8.4.2 Request an ED Measurement

There are two ways implemented in the AT86RF230 to initiate an ED measurement:

- Manually, by writing an arbitrary value to register 0x07 (PHY_ED_LEVEL), or
- Automatically, by detecting a valid SFD of an incoming frame.

For manual measurement it is recommended to start the ED measurement while being in states RX_ON or BUSY_RX.

For automated measurement the AT86RF230 starts the ED measurement if an SFD field is detected. A valid SFD detection is signalized by an RX_START interrupt and the register 0x07 (PHY_ED_LEVEL) is cleared to 0.

Thus by using Basic Operating Mode, a valid ED value from the currently received frame is accessible 140 µs after the RX_START interrupt until a new RX_START interrupt is generated by the next incoming frame or until another ED measurement is initiated manually.

By using the Extended Operating Mode, the RX_START interrupt is always masked and cannot be used as timing reference. A successful frame reception is only signalized by the TRX_END interrupt. The minimum time span between a TRX_END interrupt and a following SFD detection is 96 µs. The ED value needs to be read within this period of time; otherwise, it could be overwritten by the next measurement cycle.

The value of the register 0x07 (PHY_ED_LEVEL) is always 0 if the AT86RF230 is not in any of the RX state

8.4.3 Data Interpretation

The PHY_ED_LEVEL is an 8-bit register. The ED value of the AT86RF230 radio transceiver has a valid range from 0 to 84 with a resolution of 1 dB. All other values do not occur. If zero is read from the PHY_ED_LEVEL register, this indicates that the measured energy is less than -91 dBm (see parameter 9.7.16). Due to environmental conditions (temperature, voltage, semiconductor parameters, etc.) the computed energy value has an accuracy of ±5 dBm, this is to be considered as constant offset over the measurement range.

8.4.4 Register Description

Table 8-3. PHY_ED_LEVEL (0x07) - Energy Detection Level

Bit	Field Name	Reset	R/W	Comments
7:0	ED_LEVEL	0	R	ED level for current channel. The min. ED value (0) indicates receiver power less than or equal to RSSI_BASE_VAL. The range is 84 dB with a resolution of 1 dB and an absolute accuracy of ±5 dB.

8.5 Received Signal Strength Indicator (RSSI)

The Received Signal Strength Indicator main features are:

- Minimum RSSI sensitivity is -91 dBm (RSSI_BASE_VAL)
- Dynamic range is 81 dB
- Tolerance within gain step is ±5 dB
- Minimum RSSI value is 0
- Maximum RSSI value is 28

8.5.1 Overview

The RSSI is a 5-bit value indicating the receive power, in steps of 3 dB. The RSSI provides the basis for ED measurement.

8.5.2 Reading RSSI

Using the Basic Operating Mode, the RSSI value is valid at any RX state, and is updated every 2 µs. The current RSSI value is stored to the PHY_RSSI register.

8.5.3 Data Interpretation

The PHY_RSSI is an 8-bit register, however, the value is represented in the lowest 5 bits [4:0] and the range is 0 – 28.

An RSSI value of 0 indicates an RF input power of < -91 dBm. For an RSSI value in the range of 1 to 28, the RF input power can be calculated as follows:

$$P_{RF} = RSSI\_BASE\_VAL + 3 \cdot (RSSI - 1)$$

8.5.4 Register Description

Table 8-4 PHY_RSSI (0x06) – Received Signal Strength Indication

Bit	Field Name	Reset	R/W	Comments
7:5		0	R	Reserved
4:0	RSSI	0	R	0: RX input level < RSSI_BASE_VAL 28: RX input level ≤ -10 dBm RSSI is a linear curve on a logarithmic input power scale (dBm) with a 3 dB step width.

8.6 Link Quality Indication (LQI)

The main features of the Link Quality Indication module are:

- LQI values ranging from 0 to 255
- Uniform resolution

8.6.1 Overview

IEEE 802.15.4-2003 defines the LQI measurement as a characterization of the strength and/or quality of a received packet. The LQI measurement of the AT86RF230 is implemented as a characterization of both the quality and signal strength. The LQI measurement is an average correlation value of multiple symbols that is calculated for each received packet with an integer ranging from 0 to 255

8.6.2 Request an LQI Measurement

The LQI byte can be obtained after a frame has been received by the radio transceiver. One additional byte is attached to the received frame containing the LQI value. This information can be read as an extra byte from the Frame Buffer (see section 8.3). The LQI byte can not be uploaded before the TRX_END interrupt, it is first readable 32 µs after the IRQ occurrence.

8.6.3 Data Interpretation

The minimum LQI value of 0 is associated with a low signal quality, resulting from high signal distortions, and/or a signal strength that is below the receiver sensitivity. The maximum value of 255 is associated with a signal strength higher than the receiver sensitivity and a high signal quality resulting from low signal distortions. The LQI values in between these two limits are uniformly distributed. Signal distortions are mainly generated by interference and multi-path propagation.

8.7 Clear Channel Assessment (CCA)

The main features of the Clear Channel Assessment (CCA) module are:

- All 3 modes available as defined by IEEE 802.15.4-2003 in section 6.7.9
- Adjustable sensitivity of the CCA carrier sense algorithm.
- Adjustable threshold of the energy detection algorithm.

8.7.1 Overview

The CCA is used to detect a clear channel. There are three modes available:

- CCA Mode 1 Energy above threshold. CCA shall report a busy medium upon detecting any energy above the ED threshold.
- CCA Mode 2 Carrier sense only. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4-2003. This signal may be above or below the ED threshold.
- CCA Mode 3 Carrier sense with energy above threshold. CCA shall report a busy medium only upon the detection of a signal with the modulation and spreading characteristics of IEEE 802.15.4-2003 with energy above the ED threshold.

8.7.2 CCA Request

The CCA modes are configurable via register 0x08 (PHY_CC_CCA). The CCA threshold values are configurable using register 0x09 (CCA_THRES).

The 4-bit value CCA_CS_THRES of register 0x09 (CCA_THRES) can be used for fine tuning the sensitivity of the CCA carrier sense algorithm. Higher values increase the probability of clear channel detection.

The other 4-bit value CCA_ED_THRES of register 0x09 (CCA_THRES) defines the received power threshold of the “energy above threshold” algorithm. The threshold is calculated by RSSI_BASE_VAL+2·CCA_ED_THRES [dBm]. Any received power above this level is interpreted as a busy channel.

Using the Basic Operating Mode, a CCA request can be initiated manually by setting CCA_REQUEST = 1 in register 0x08 (PHY_CC_CCA), if the AT86RF230 is in any RX state. The current channel status (CCA_STATUS) and the CCA completion status (CCA_DONE) are accessible in register 0x01 (TRX_STATUS). The CCA evaluation is done over eight symbols and the result is accessible 140 µs after the request.

8.7.3 Register Description

Table 8-5. TRX_STATUS (0x01) – CCA Result

Bit	Field Name	Reset	R/W	Comments
7	CCA_DONE	0	R	0: CCA calculation in progress 1: CCA calculation done
6	CCA_STATUS	0	R	Indicates an idle channel from CCA module. 0: channel is busy 1: channel is idle
5		0	R	Reserved
4:0	TRX_STATUS	0	R	Current radio transceiver status. 0: P_ON 1: BUSY_RX 2: BUSY_TX 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 15: SLEEP 17: BUSY_RX_AACK 18: BUSY_TX_ARET 22: RX_AACK_ON 25: TX_ARET_ON 28: RX_ON_NOCLK 29: RX_AACK_ON_NOCLK 30: BUSY_RX_AACK_NOCLK 31: STATE_TRANSITION_IN_PROGRESS

Table 8-6. PHY_CC_CCA (0x08) – CCA Mode Configuration and CCA request

Bit	Field Name	Reset	R/W	Comments
7	CCA_REQUEST	0	R/W	1: starts a CCA check (CCA.request) read value always returns with 0
6:5	CCA_MODE	1	R/W	CCA Mode: 0: Reserved 1: Mode 1, energy above threshold 2: Mode 2, carrier sense only 3: Mode 3, carrier sense with energy above threshold
4:0	CHANNEL	11	R/W	Channel: According to IEEE 802.15.4-2003 only 11 to 26 are valid. All unused values are reserved.

Channel Mapping	
Channel Number	Frequency [MHz]
11	2405
12	2410
13	2415
14	2420
15	2425
16	2430
17	2435
18	2440
19	2445
20	2450
21	2455
22	2460
23	2465
24	2470
25	2475
26	2480

Table 8-7. CCA_THRES (0x09) – CCA_ED and CCA_CS Threshold

Bit	Field Name	Reset	R/W	Comments
7:4	CCA_CS_THRES	12	R/W	Threshold for CCA_CS
3:0	CCA_ED_THRES	7	R/W	An ED value above the threshold indicates a busy channel during a CCA_ED measurement.

8.8 Voltage Regulators (AVREG, DVREG)

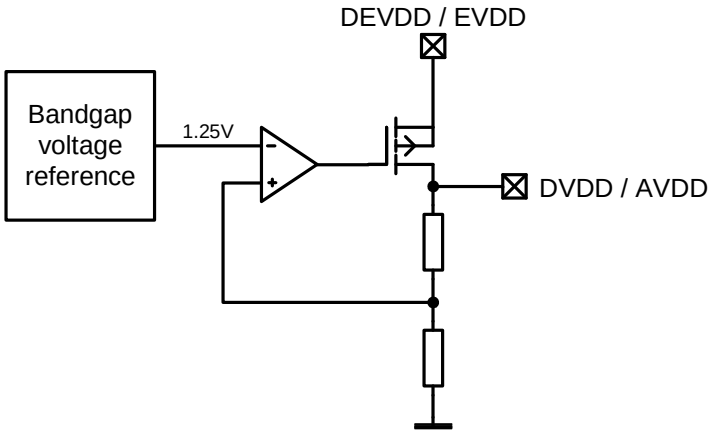
The main features of the Voltage Regulator modules are:

- Bandgap stabilized 1.8V supply for analog and digital domain.
- Low dropout (LDO) voltage regulator
- Configurable for usage of external voltage regulator

8.8.1 Overview

The internal voltage regulators supply a stable voltage to the AT86RF230. The AVREG provides the regulated 1.8V supply voltage for the analog section and the DVREG supplies the 1.8V supply voltage for the digital section. A simplified schematic of the internal voltage regulator is shown in **Figure 8-3**.

Figure 8-3. Simplified Schematic of AVREG/DVREG



8.8.2 Configure the Voltage Regulators

The voltage regulators can be configured by the register 0x10 (VREG_CTRL).

It is recommended to use the internal regulators, but it is also possible to supply the low voltage domains by an external voltage source. For this configuration, the internal regulators need to be switched off by setting the register bits to the values AVREG_EXT = 1 and DVREG_EXT = 1. A regulated external supply voltage of 1.8V needs to be connected to the pins DVDD and AVDD. When turning on the external supply, ensure a sufficiently long stabilization time before interacting with the AT86RF230.

8.8.3 Data Interpretation

The status bit values AVDD_OK = 1 and DVDD_OK = 1 indicate an enabled and stable internal supply voltage. Reading 0 indicates a disabled or unstable internal supply voltage.

8.8.4 Register Description

Table 8-8. VREG_CTRL (0x10) - Voltage Regulator Control

Bit	Field Name	Reset	R/W	Comments
7	AVREG_EXT	0	R/W	0: use internal analog voltage regulator 1: use external voltage regulator
6	AVDD_OK	0	R	0: internal analog voltage regulator is disabled 1: internal analog voltage regulator is enabled and stable
5:4		0	R/W	Reserved
3	DVREG_EXT	0	R/W	0: use internal digital voltage regulator 1: use external voltage regulator
2	DVDD_OK	0	R	0: internal digital voltage regulator is disabled 1: internal digital voltage regulator is enabled and stable
1:0		0	R/W	Reserved

8.9 Battery Monitor (BATMON)

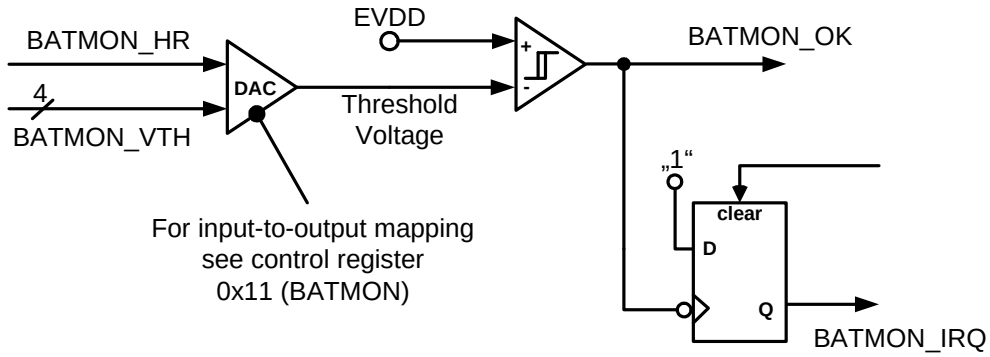
The main features of the battery monitor are:

- Programmable voltage threshold range: 1.7V to 3.675V
- Battery low voltage interrupt

8.9.1 Overview

The battery monitor (BATMON) detects and indicates a low supply voltage. This is done by comparing the voltage on the external supply pin (EVDD) with a programmable internal threshold voltage. A simplified schematic of the BATMON with the most important input and output signals is shown in **Figure 8-4**.

Figure 8-4. Simplified Schematic of BATMON



8.9.2 Configuring BATMON

The BATMON can be configured using the register 0x11 (BATMON). Register bits BATMON_VTH sets the threshold voltage. It is programmable with a resolution of 75 mV in the upper voltage range (BATMON_HR = 1) and with a resolution of 50 mV in the lower voltage range (BATMON_HR = 0).

8.9.3 Data Interpretation

The signal bit BATMON_OK of register 0x11 (BATMON) indicates the current value of the battery voltage:

- If BATMON_OK = 0, the battery voltage is lower than the threshold voltage
- If BATMON_OK = 1, the battery voltage is higher than the threshold voltage

The interrupt IRQ_7 (BAT_LOW) is automatically generated if the battery voltage drops below the programmed threshold (see control register 0x0E and 0x0F). The interrupt is issued only if BATMON_OK changes from 1 to 0.

No interrupt is generated when:

- The battery voltage is under the default 1.8V threshold at power up (BATMON_OK was never 1), or
- A new threshold is set, which is still above the current supply voltage (BATMON_OK remains 0).

After setting a new threshold, the value BATMON_OK should be read out to verify the current supply voltage value.

When the battery voltage is close to the programmed threshold voltage, noise or temporary voltage drops may generate unwanted interrupts. To avoid this:

- Disable the IRQ_7 (BAT_LOW) in register 0x0E (IRQ_MASK) and treat the battery as empty, or
- Set a lower threshold value.

Note: The battery monitor is inactive during P_ON and SLEEP states, see control register 0x01 (TRX_STATUS).

8.9.4 Register Description

Table 8-9. BATMON (0x11) – Battery Monitor Configuration

Bit	Field Name	Reset	R/W	Comments		
7:6		0	R	Reserved		
5	BATMON_OK	0	R	Result of battery monitor: 0: V_{DD} < BATMON_VTH 1: V_{DD} > BATMON_VTH		
4	BATMON_HR	0	R/W	High range switch (mapping see BATMON_VTH)		
3:0	BATMON_VTH	2	R/W	Threshold voltage:		
				BATMON_VTH Mapping		
				Value	Voltage [V] BATMON_HR = 1	Voltage [V] BATMON_HR = 0
				0	2.550	1.70
				1	2.625	1.75
				2	2.700	1.80
				3	2.775	1.85
				4	2.850	1.90
				5	2.925	1.95
				6	3.000	2.00
				7	3.075	2.05
				8	3.150	2.10
				9	3.225	2.15
				10	3.300	2.20
				11	3.375	2.25
				12	3.450	2.30
				13	3.525	2.35
				14	3.600	2.40
				15	3.675	2.45

8.10 Crystal Oscillator (XOSC)

The main crystal oscillator features are:

- 16 MHz amplitude controlled crystal oscillator
- 500 µs typical settling time
- Integrated trimming capacitance array
- Programmable clock output (CLKM)

8.10.1 Overview

The crystal oscillator generates the reference frequency for the AT86RF230. All other internally generated frequencies of the radio transceiver are derived from this unique frequency. Therefore, the overall system performance is mainly based on the accuracy of this reference frequency. The external components of the crystal oscillator should be selected carefully and the related board layout should be done meticulously (see section 5).

The register 0x12 (XOSC_CTRL) provides access to the control signals of the oscillator. Two operating modes are supported. It is recommended to use the integrated oscillator setup as described in **Figure 8-5**, nevertheless a reference frequency can be fed to the internal circuitry by using an external clock reference as shown in **Figure 8-6**.

8.10.2 Integrated Oscillator Setup

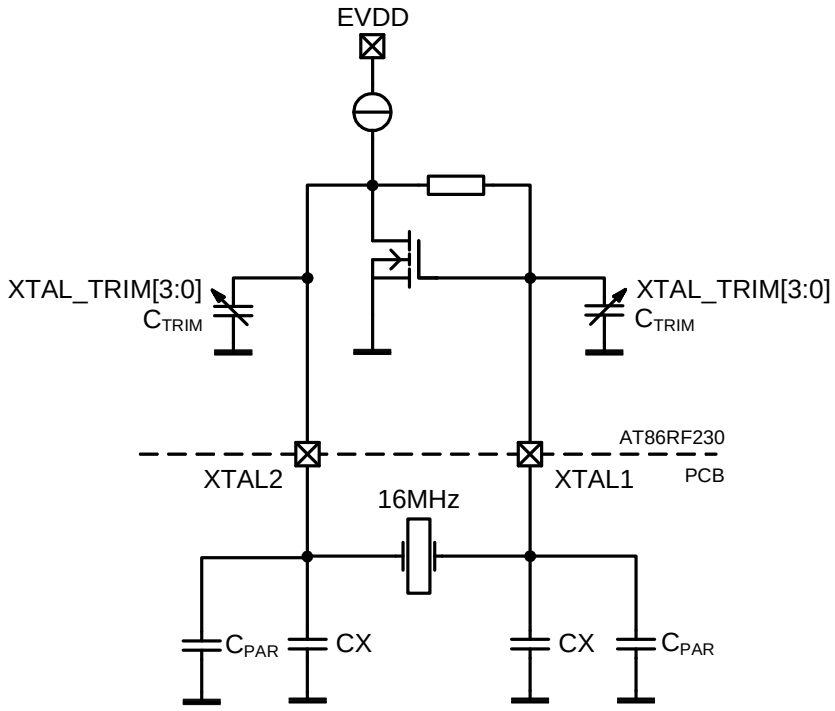
Using the internal oscillator, the oscillation frequency strongly depends on the load capacitance between the crystal pins XTAL1 and XTAL2. The total load capacitance must be equal to the specified load capacitance CL of the crystal itself. It consists of the external capacitors CX and parasitic capacitances connected to the XTAL nodes. In **Figure 8-5**, all parasitic capacitances, such as PCB stray capacitances and the pin input capacitance, are summarized to C_{PAR}. Additional internal trimming capacitors C_{TRIM} are available. Any value in the range from 0 pF to 4.8 pF with a 0.3 pF resolution is selectable using XTAL_TRIM of register 0x12 (XOSC_CTRL). To calculate the total load capacitance, the following formula can be used $CL = 0.5 \cdot (CX + C_{TRIM} + C_{PAR})$.

The trimming capacitors provide the possibility of reducing frequency deviations caused by production process variations or by external components tolerances. Note that the oscillation frequency can be reduced only by increasing the trimming capacitance. The frequency deviation caused by one step of C_{TRIM} decreases with increasing crystal load capacitor values.

A magnitude control circuit is included to ensure stable operation under different operating conditions and for different crystal types. A high current during the amplitude build-up phase guarantees a low start-up time. At stable operation, the current is reduced to the amount necessary for a robust operation. This also keeps the drive level of the crystal low.

Generally, crystals with a higher load capacitance are less sensitive to parasitic pulling effects caused by external component variations or by variations of board and circuit parasitics. On the other hand, a larger crystal load capacitance results in a longer start-up time and a higher steady state current consumption.

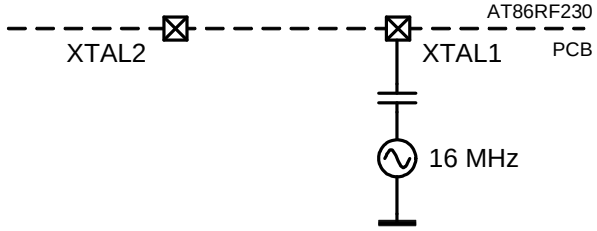
Figure 8-5. Simplified XOSC Schematic with External Components



8.10.3 External Reference Frequency Setup

When using an external reference frequency, the signal needs to be connected to pin XTAL1 as indicated in **Figure 8-6** and the register XTAL_MODE of register 0x12 (XOSC_CTRL) need to be set to the external oscillator mode. The oscillation peak-to-peak amplitude shall be 400 mV, but not larger than 500 mV.

Figure 8-6. Setup for Using an External Frequency Reference



8.10.4 Master Clock Signal Output (CLKM)

The generated reference clock signal can be fed to a microcontroller using the CLKM pin. The internal 16 MHz raw clock is divided by an internal prescaler. Thus, clock frequencies of 16 MHz, 8 MHz, 4 MHz, 2 MHz or 1 MHz can be supplied by the CLKM pin.

The CLKM frequency and pin driver strength is configurable in register 0x03 (TRX_CTRL_0). There are two ways to change the CLKM frequency. If CLKM_SHA_SEL = 0, changing the register bits CLKM_CTRL immediately affects the CLKM frequency. Otherwise (CLKM_SHA_SEL = 1) the new clock frequency is supplied when leaving the SLEEP state the next time.

To reduce power consumption and spurious emissions, it is recommended to turn off the CLKM clock when not in use.

8.10.5 Register Description

Table 8-10. XOSC_CTRL (0x12) – Crystal Oscillator Control

Bit	Field Name	Reset	R/W	Comments
7:4	XTAL_MODE	15	R/W	XTAL Modes: 0: switched off 4: external signal 15: internal oscillator All other modes are reserved and should not be used.
3:0	XTAL_TRIM	0	R/W	Binary coded capacitance array for XTAL trimming. Values: 0 pF, 0.3 pF, …, 4.8 pF

Table 8-11. TRX_CTRL_0 (0x03) – CLKM Pin Configuration

Bit	Field Name	Reset	R/W	Comments
7:6	PAD_IO	0	R/W	Set the output driver current of digital pads (except CLKM pad). 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
5:4	PAD_IO_CLKM	1	R/W	Set the output driver current of CLKM. 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
3	CLKM_SHA_SEL	1	R/W	Shadow the CLKM_CTRL clock changes. If the mode is enabled, changes to the CLKM_CTRL bits take effect only when the radio transceiver leaves the SLEEP state. 0: disable (immediate change) 1: enable (shadow)
2:0	CLKM_CTRL	1	R/W	Controls the clock frequency at the CLKM pad. 0: no clock 1: 1 MHz 2: 2 MHz 3: 4 MHz 4: 8 MHz 5: 16 MHz 6: no clock 7: no clock

8.11 Frequency Synthesizer (PLL)

The main PLL features are:

- Fully integrated fractional-N synthesizer
- Generate RX/TX frequencies for all IEEE 802.15.4-2003 2.4 GHz channels derived from a 16 MHz crystal based reference frequency
- Autonomous calibration loops for stable operation within the operating range
- Two PLL-interrupts for status indication

8.11.1 Overview

The synthesizer of the AT86RF230 is implemented as a fractional-N PLL. The PLL is fully integrated and configurable by registers 0x08 (PHY_CC_CCA), 0x1A (PLL_CF) and 0x1B (PLL_DCU).

The PLL is turned on when entering the state PLL_ON and stays on in all receive and transmit states. In state PLL_ON and all receive states, the PLL settles to the RX frequency according to the adjusted channel center frequency in register 0x08 (PHY_CC_CCA).

Two calibration loops ensure correct PLL functionality within the specified operating limits.

8.11.2 Calibration Loops

The center frequency control loop ensures a correct center frequency of the VCO for the currently programmed channel.

The delay calibration unit compensates the phase errors inherent in fractional-N PLLs. Using this technique, unwanted spurious frequency components beside the RF carrier are suppressed, and the PLL behaves similar to an integer-N PLL.

Both calibration routines are initiated automatically when the PLL is turned on. Additionally, the center frequency calibration is running when the PLL is programmed to a different channel (register bits CHANNEL in register 0x08).

If the PLL operates for a long time on the same channel or the operating temperature changes significantly, the control loops should be initiated manually. The recommended calibration interval is 5 min.

Both calibration loops can be initiated manually by setting PLL_CF_START = 1 of register 0x1A (PLL_CF) and register bit PLL_DCU_START = 1 of register 0x1B (PLL_DCU). To start the calibrations routines the device should be in state PLL_ON. The completion of the center frequency tuning is indicated by a PLL_LOCK interrupt.

8.11.3 PLL Interrupts

There are two different interrupts that indicate PLL status (see register 0x0F). The PLL_LOCK interrupt indicates that the PLL has locked. The PLL_UNLOCK interrupt indicates an unexpected unlock condition. A PLL_LOCK interrupt clears any preceding PLL_UNLOCK interrupt automatically and vice versa.

A PLL_LOCK interrupt occurs in the following situations:

- State change from TRX_OFF to PLL_ON / RX_ON
- Channel change in states PLL_ON / RX_ON

The state transition from BUSY_TX to PLL_ON can also initiate a PLL_LOCK interrupt, due to the PLL settling back to the RX frequency.

Any other occurrences of PLL interrupts indicate erroneous behaviour and require checking of the actual device status.

8.11.4 Register Description

Table 8-12. PLL_CF (0x1A) – PLL Center Frequency Calibration

Bit	Field Name	Reset	R/W	Comments
7	PLL_CF_START	0	R/W	1: Initiates PLL center frequency calibration cycle If frequency calibration is finished, read value is 0
6:4		5	R/W	Reserved
3:0		15	R/W	Reserved

Table 8-13. PLL_DCU (0x1B – PLL Delay Calibration

Bit	Field Name	Reset	R/W	Comments
7	PLL_DCU_START	0	R/W	1: Initiates PLL delay cell calibration cycle If delay cell calibration is finished, read value is 0
6		0	R	Reserved
5:0		32	R/W	Reserved

8.12 Automatic Filter Tuning (FTN)

The filter-tuning unit is a separate block within the AT86RF230. The filter-tuning result is used to provide a correct SSBF transfer function and PLL loop-filter time constant independent of temperature effects and part-to-part variations.

A calibration cycle is initiated automatically when entering the TRX_OFF state from the SLEEP, RESET or P_ON states.

9 Technical Parameters

9.1 Absolute Maximum Ratings

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 9-1. Absolute Maximum Ratings

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.1.1	Storage temperature	T_{stor}	-50		150	°C	
9.1.2	Lead temperature	T_{lead}			260	°C	T = 10s (soldering profile compliant with IPC/JEDEC J-STD-020B)
9.1.3	ESD robustness	V_{ESD}	4 750			kV V	Compl. to [2] Compl. to [3]
9.1.4	Input RF level	P_{RF}			+14	dBm	
9.1.5	Voltage on all pins (except pins 13, 14, 29)		-0.3		V_{DD}+0.3 ≤ 4.0	V	
9.1.6	Voltage on pins 13, 14, 29		-0.3		2.0	V	

9.2 Recommended Operating Range

Table 9-2. Operating Range

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.2.1	Operating temperature range	T_{op}	-40		+85	°C	
9.2.2	Supply voltage	V_{DD}	1.8	3.0	3.6	V	
9.2.3	Supply voltage (on pins 13, 14, 29)	$V_{DD1.8}$	1.65	1.8	1.95	V	When using external voltage regulators (see section 8.8).

9.3 Digital Pin Specifications

Test Conditions (unless otherwise stated): T_{op} = 25°C

Table 9-3. Digital Pin Specifications

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.3.1	High level input voltage	V_{IH}	V_{DD} – 0.4			V	
9.3.2	Low level input voltage	V_{IL}			0.4	V	
9.3.3	High level output voltage	V_{OH}	V_{DD} – 0.4			V	For all output driver strengths defined in TRX_CTRL_0
9.3.4	Low level output voltage	V_{OL}			0.4	V	For all output driver strengths defined in TRX_CTRL_0

The capacitive load should not be larger than 50 pF for all I/Os when using the default driver strength settings. Generally, large load capacitances increase the overall current consumption.

9.4 Digital Interface Timing Specifications

Test Conditions (unless otherwise stated): V_{DD} = 3V, T_{op} = 25°C

Table 9-4. Digital Interface Timing Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.4.1	SCLK frequency (synchronous mode)				8	MHz	
9.4.2	SCLK frequency (asynchronous mode)				7.5	MHz	
9.4.3	$\overline{SEL}$ low to MISO active	t1			180	ns	
9.4.4	SCLK to MISO out	t2	48			ns	data hold time
9.4.5	MOSI setup time	t3	10			ns	
9.4.6	MOSI hold time	t4	10			ns	
9.4.7	LSB last byte to MSB next byte	t5			250	ns	
9.4.8	$\overline{SEL}$ high to MISO tristate	t6			10	ns	
9.4.9	SLP_TR pulse width	t7	65			ns	TX start trigger
9.4.10	SPI idle time	t8	250			ns	Idle time between consecutive SPI accesses
9.4.11	Reset pulse width		625			ns	≥ 10 clock cycles at 16 MHz
9.4.12	Output clock frequency (CLKM)	f_{CLKM}		0 1 2 4 8 16		MHz MHz MHz MHz MHz MHz	Programmable in register TRX_CTRL_0

9.5 General RF Specifications

Test Conditions (unless otherwise stated): V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see **Figure 5-1**

Table 9-5: General RF Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.5.1	Frequency range	f	2405		2480	MHz	
9.5.2	Bit rate	f_{bit}		250		kbit/s	As specified in [1]
9.5.3	Chip rate	f_{chip}		2000		kchip/s	As specified in [1]
9.5.4	Reference oscillator frequency	f_{clk}		16		MHz	
9.5.5	Reference oscillator settling time			0.5	1	ms	Leaving SLEEP state to clock available at pin CLKM
9.5.6	Reference frequency accuracy for proper functionality		-60		+60	ppm	±40 ppm is required by [1]
9.5.7	TX signal 20 dB bandwidth	B_{20dB}		2.8		MHz	

9.6 Transmitter Specifications

Test Conditions (unless otherwise stated): V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see **Figure 5-1**

Table 9-6. TX Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.6.1	Nominal output power	P_{TX}	0	3	6	dBm	Max. value
9.6.2	Output power range			20		dB	16 steps (register PHY_TX_PWR)
9.6.3	Output power accuracy				±3	dB	
9.6.4	TX Return loss			10		dB	100Ω differential impedance, P_{TX} = 3 dBm
9.6.5	EVM			8		%rms	
9.6.6	Harmonics 2nd harmonic 3rd harmonic			 -38 -45		 dBm dBm	
9.6.7	Spurious emissions 30 – ≤ 1000 MHz >1 – 12.75 GHz 1.8 – 1.9 GHz 5.15 – 5.3 GHz				 -36 -30 -47 -47	 dBm dBm dBm dBm	Complies with EN 300 328/440, FCC-CFR-47 part 15, ARIB STD-66, RSS-210

9.7 Receiver Specifications

Test Conditions (unless otherwise stated): V_{DD} = 3V, f = 2.45 GHz, T_{op} = 25°C, Measurement setup see **Figure 5-1**

Table 9-7. RX Parameters

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.7.1	Receiver sensitivity			-101		dBm	AWGN channel, PER ≤ 1%, PSDU length of 20 octets
9.7.2	Return loss			10		dB	100Ω differential impedance
9.7.3	Noise figure	NF		6		dB	
9.7.4	Maximum RX input level			10		dBm	PER ≤ 1%, PSDU length of 20 octets
9.7.5	Adjacent channel rejection -5 MHz			34		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
9.7.6	Adjacent channel rejection +5 MHz			36		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
9.7.7	Alternate adjacent channel rejection -10 MHz			52		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
9.7.8	Alternate adjacent channel rejection +10 MHz			53		dBm	PER ≤ 1%, PSDU length of 20 octets, P_{RF} = -82 dBm
9.7.9	Spurious emissions LO leakage 30 – ≤ 1000 MHz >1 – 12.75 GHz			 -75	 -57 -47	 dBm dBm dBm	

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.7.10	TX/RX carrier frequency offset tolerance		-300		300	kHz	Sensitivity loss < 2 dB; equals 120 ppm ([1] requires 80 ppm)
9.7.11	3rd-order intercept point	IIP3		-9		dB	At maximum gain Offset freq. interf. 1 = 5 MHz Offset freq. interf. 2 = 10 MHz
9.7.12	2nd-order intercept point	IIP2		24		dB	At maximum gain Offset freq. interf. 1 = 60 MHz Offset freq. interf. 2 = 62 MHz
9.7.13	RSSI accuracy absolute		-5		5	dB	Tolerance within gain step
9.7.14	RSSI dynamic range			81		dB	
9.7.15	RSSI resolution			3		dB	
9.7.16	RSSI_BASE_VAL			-91		dBm	Minimum RSSI sensitivity
9.7.17	Minimum RSSI value			0			P_{RF} < RSSI_BASE_VAL
9.7.18	Maximum RSSI value			28			P_{RF} ≥ -10 dBm

9.8 Current Consumption Specifications

Test Conditions (unless otherwise stated): V_{DD} = 3V, T_{op} = 25°C, CLKM = OFF, Measurement setup see **Figure 5-1**

Table 9-8. Current Consumption

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.8.1	Supply current transmit state	I_{BUSY_TX}		17 15 13 10		mA mA mA mA	P_{TX} = 3 dBm P_{TX} = 1 dBm P_{TX} = -3 dBm P_{TX} = -17 dBm (the current consumption will be reduced by approx. 2 mA at V_{DD} = 1.8V for each output power level)
9.8.2	Supply current receive state	I_{RX_ON}		16		mA	State: RX_ON
9.8.3	Supply current TRX_OFF state	I_{TRX_OFF}		1.7		mA	State: TRX_OFF
9.8.4	Supply current SLEEP state	I_{SLEEP}		0.1		µA	State: SLEEP

9.9 Crystal Parameter Requirements

Table 9-9. Crystal Parameter Requirements

No	Parameter	Symbol	Min	Typ	Max	Unit	Conditions/Notes
9.9.1	Crystal frequency	f_0		16		MHz	
9.9.2	Load capacitance	C_L	8		14	pF	
9.9.3	Static capacitance	C_0			7	pF	
9.9.4	Series resistance	R_1			100	Ω	

10 Register Reference

The AT86RF230 provides a register space of 64 8-bit registers, which is used to configure, control and monitor the radio transceiver.

Note: All registers not mentioned within the following table are reserved for internal use and must not be overwritten. When writing to a register, any reserved bits shall be overwritten only with their reset value.

Table 10-1. Configuration Registers Overview

Reg.-Addr.	Register Name	Description
0x01	TRX_STATUS	Radio transceiver status, CCA result
0x02	TRX_STATE	State control
0x03	TRX_CTRL_0	Driver current and output clock setting
0x05	PHY_TX_PWR	TX power setting
0x06	PHY_RSSI	RSSI value
0x07	PHY_ED_LEVEL	RX energy level
0x08	PHY_CC_CCA	CCA mode configuration, CCA request, channel setting
0x09	CCA_THRES	CCA_ED and CCA_CS threshold
0x0E	IRQ_MASK	Interrupt mask
0x0F	IRQ_STATUS	Interrupt status
0x10	VREG_CTRL	Voltage regulator control
0x11	BATMON	Battery monitor control
0x12	XOSC_CTRL	Crystal oscillator control
0x1A	PLL_CF	PLL center frequency calibration
0x1B	PLL_DCU	PLL delay calibration
0x1C	PART_NUM	Part ID
0x1D	VERSION_NUM	Version ID
0x1E	MAN_ID_0	Manufacturer ID, lower 8 bits
0x1F	MAN_ID_1	Manufacturer ID, higher 8 bits
0x20	SHORT_ADDR_0	Short address for address recognition
0x21	SHORT_ADDR_1	Short address for address recognition
0x22	PAN_ID_0	PAN address for address recognition
0x23	PAN_ID_1	PAN address for address recognition
0x24	IEEE_ADDR_0	Current node IEEE address for address recognition
0x25	IEEE_ADDR_1	Current node IEEE address for address recognition
0x26	IEEE_ADDR_2	Current node IEEE address for address recognition
0x27	IEEE_ADDR_3	Current node IEEE address for address recognition
0x28	IEEE_ADDR_4	Current node IEEE address for address recognition
0x29	IEEE_ADDR_5	Current node IEEE address for address recognition
0x2A	IEEE_ADDR_6	Current node IEEE address for address recognition
0x2B	IEEE_ADDR_7	Current node IEEE address for address recognition
0x2C	XAH_CTRL	Retries value control
0x2D	CSMA_SEED_0	CSMA seed value
0x2E	CSMA_SEED_1	CSMA seed value

Table 10-2. 0x01 - TRX_STATUS

Bit	Field Name	Reset	R/W	Comments
7	CCA_DONE	0	R	0: CCA calculation in progress 1: CCA calculation done
6	CCA_STATUS	0	R	Indicates an idle channel from CCA module. 0: channel is busy 1: channel is idle
5		0	R	Reserved
4:0	TRX_STATUS	0	R	Current radio transceiver status. 0: P_ON 1: BUSY_RX 2: BUSY_TX 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 15: SLEEP 17: BUSY_RX_AACK 18: BUSY_TX_ARET 22: RX_AACK_ON 25: TX_ARET_ON 28: RX_ON_NOCLK 29: RX_AACK_ON_NOCLK 30: BUSY_RX_AACK_NOCLK 31: STATE_TRANSITION_IN_PROGRESS

Note: A register read resets the CCA_STATUS bit and the CCA_DONE bit if a CCA calculation was done (CCA_DONE = 1).

Table 10-3. 0x02 - TRX_STATE

Bit	Field Name	Reset	R/W	Comments
7:5	TRAC_STATUS	0	R	0: SUCCESS 3: CHANNEL_ACCESS_FAILURE 5: NO_ACK All other values are reserved.
4:0	TRX_CMD	0	R/W	Radio transceiver control commands: 0: NOP 2: TX_START 3: FORCE_TRX_OFF 6: RX_ON 8: TRX_OFF (Clock State) 9: PLL_ON (TX_ON) 22: RX_AACK_ON 25: TX_ARET_ON All other values are mapped to NOP.

Note: TRX_CMD = 0 after power on reset (POR).
Frame transmission starts 16 µs after TX_START command.

Table 10-4. 0x03 - TRX_CTRL_0

Bit	Field Name	Reset	R/W	Comments
7:6	PAD_IO	0	R/W	Set the output driver current of digital pads (except CLKM pad). 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
5:4	PAD_IO_CLKM	1	R/W	Set the output driver current of CLKM. 0: 2 mA 1: 4 mA 2: 6 mA 3: 8 mA
3	CLKM_SHA_SEL	1	R/W	Shadow the CLKM_CTRL clock changes. If the mode is enabled, changes to the CLKM_CTRL bits take effect only when the radio transceiver leaves the SLEEP state. 0: disable (immediate change) 1: enable (shadow)
2:0	CLKM_CTRL	1	R/W	Controls the clock frequency at the CLKM pad. 0: no clock 1: 1 MHz 2: 2 MHz 3: 4 MHz 4: 8 MHz 5: 16 MHz 6: no clock 7: no clock

Table 10-5. 0x05 - PHY_TX_PWR

Bit	Field Name	Reset	R/W	Comments
7	TX_AUTO_CRC_ON	0	R/W	AUTO_CRC mode: 0: disable 1: enable
6:4		0	R	Reserved
3:0	TX_PWR	0	R/W	**TX Power Mapping**

TX Power Setting	Output Power [dBm]
0	3.0
1	2.6
2	2.1
3	1.6
4	1.1
5	0.5
6	-0.2
7	-1.2
8	-2.2
9	-3.2
10	-4.2
11	-5.2
12	-7.2
13	-9.2
14	-12.2
15	-17.2

Table 10-6. 0x06 - PHY_RSSI

Bit	Field Name	Reset	R/W	Comments
7:5		0	R	Reserved
4:0	RSSI	0	R	0: RX input level < RSSI_BASE_VAL 28: RX input level ≥ -10 dBm RSSI is a linear curve on a logarithmic input power scale (dBm) with a 3 dB step width.

Table 10-7. 0x07 - PHY_ED_LEVEL

Bit	Field Name	Reset	R/W	Comments
7:0	ED_LEVEL	0	R	ED level for current channel. The min. ED value (0) indicates receiver power less than or equal to RSSI_BASE_VAL. The range is 84 dB with a resolution of 1 dB and an absolute accuracy of ±5 dB.

Note: A write access initiates the ED measurement (ED.request).

Table 10-8. 0x08 - PHY_CC_CCA

Bit	Field Name	Reset	R/W	Comments
7	CCA_REQUEST	0	R/W	1: starts a CCA check (CCA.request) Read value always returns with 0
6:5	CCA_MODE	1	R/W	CCA Mode: 0: Reserved 1: Mode 1, energy above threshold 2: Mode 2, carrier sense only 3: Mode 3, carrier sense with energy above threshold
4:0	CHANNEL	11	R/W	Channel: According to IEEE 802.15.4-2003 only 11 to 26 are valid. All unused values are reserved.

Channel Mapping

Channel Number	Frequency [MHz]
11	2405
12	2410
13	2415
14	2420
15	2425
16	2430
17	2435
18	2440
19	2445
20	2450
21	2455
22	2460
23	2465
24	2470
25	2475
26	2480

Table 10-9. 0x09 - CCA_THRES

Bit	Field Name	Reset	R/W	Comments
7:4	CCA_CS_THRES	12	R/W	Threshold for CCA_CS
3:0	CCA_ED_THRES	7	R/W	An ED value above the threshold signals a busy channel during a CCA_ED measurement.

Note: CCA_ED_THRES: The CCA_ED request indicates a busy channel, if the measured receive power is above RSSI_BASE_VAL + 2*CCA_ED_THRES[dB].

Table 10-10. 0x0E - IRQ_MASK

Bit	Field Name	Reset	R/W	Comments
7:0	IRQ_MASK	255	R/W	Mask register for IRQs. If bit is set to high, then the IRQ is enabled. If bit is set to low, then the IRQ is disabled. IRQ_MASK[7] corresponds to IRQ_7. IRQ_MASK[0] corresponds to IRQ_0.

Note: The occurrence of an interrupt is signaled over the IRQ wire.

Table 10-11. 0x0F - IRQ_STATUS

Bit	Field Name	Reset	R/W	Comments	
7	IRQ_7	0	R	BAT_LOW:	signals low battery
6	IRQ_6	0	R	TRX_UR:	signals a FIFO underrun
5		0	R	Reserved	
4		0	R	Reserved	
3	IRQ_3	0	R	TRX_END:	signals end of frame (transmit and receive)
2	IRQ_2	0	R	RX_START:	signals beginning of receive frame
1	IRQ_1	0	R	PLL_UNLOCK:	PLL goes from lock to unlock state
0	IRQ_0	0	R	PLL_LOCK:	PLL goes from unlock to lock state

Note: The occurrence of an interrupt is signaled over the IRQ wire. A read access resets the interrupt bits.

Table 10-12. 0x10 - VREG_CTRL

Bit	Field Name	Reset	R/W	Comments
7	AVREG_EXT	0	R/W	0: use internal analog voltage regulator 1: use external voltage regulator
6	AVDD_OK	0	R	0: internal analog voltage regulator is disabled 1: internal analog voltage regulator is enabled and stable
5:4		0	R/W	Reserved
3	DVREG_EXT	0	R/W	0: use internal digital voltage regulator 1: use external voltage regulator
2	DVDD_OK	0	R	0: internal digital voltage regulator is disabled 1: internal digital voltage regulator is enabled and stable
1:0		0	R/W	Reserved

Table 10-13. 0x11 - BATMON

Bit	Field Name	Reset	R/W	Comments		
7:6		0	R	Reserved		
5	BATMON_OK	0	R	Result of battery monitor: 0: V_{DD} < BATMON_VTH 1: V_{DD} > BATMON_VTH		
4	BATMON_HR	0	R/W	High range switch (mapping see BATMON_VTH)		
3:0	BATMON_VTH	2	R/W	Threshold voltage:		
				BATMON_VTH Mapping		
				Value	Voltage [V] BATMON_HR = 1	Voltage [V] BATMON_HR = 0
				0	2.550	1.70
				1	2.625	1.75
				2	2.700	1.80
				3	2.775	1.85
				4	2.850	1.90
				5	2.925	1.95
				6	3.000	2.00
				7	3.075	2.05
				8	3.150	2.10
				9	3.225	2.15
				10	3.300	2.20
				11	3.375	2.25
				12	3.450	2.30
				13	3.525	2.35
				14	3.600	2.40
				15	3.675	2.45

Table 10-14. 0x12 - XOSC_CTRL

Bit	Field Name	Reset	R/W	Comments
7:4	XTAL_MODE	15	R/W	XTAL Modes: 0: switched off 4: external signal 15: internal oscillator All other modes are reserved and should not be used.
3:0	XTAL_TRIM	0	R/W	Binary coded capacitance array for XTAL trimming. Values: 0 pF, 0.3 pF, …, 4.8 pF

Table 10-15. 0x1A – PLL_CF

Bit	Field Name	Reset	R/W	Comments
7	PLL_CF_START	0	R/W	1: Initiates PLL center frequency calibration cycle If frequency calibration is finished, read value is 0
6:4		5	R/W	Reserved
3:0		15	R/W	Reserved

Table 10-16. 0x1B – PLL_DCU

Bit	Field Name	Reset	R/W	Comments
7	PLL_DCU_START	0	R/W	1: Initiates PLL delay cell calibration cycle If delay cell calibration is finished, read value is 0
6		0	R	Reserved
5:0		32	R/W	Reserved

Table 10-17. 0x1C - PART_NUM

Bit	Field Name	Reset	R/W	Comments
7:0	PART_NUM	2	R	The device part number. 2: AT86RF230 All other values are reserved

Table 10-18. 0x1D - VERSION_NUM

Bit	Field Name	Reset	R/W	Comments
7:0	VERSION_NUM	1	R	The device version number. 1: Revision A

Table 10-19. 0x1E - MAN_ID_0

Bit	Field Name	Reset	R/W	Comments
7:0	MAN_ID_0	31	R	JEDEC manufacturer ID is 0x0000 001F for Atmel, bits[7:0]

Table 10-20. 0x1F - MAN_ID_1

Bit	Field Name	Reset	R/W	Comments
7:0	MAN_ID_1	0	R	JEDEC manufacturer ID is 0x0000 001F for Atmel, bits[15:8]

Table 10-21. 0x20 - SHORT_ADDR_0

Bit	Field Name	Reset	R/W	Comments
7:0	SHORT_ADDR_0	0	R/W	Lower 8 bits of short address for address recognition, bits[7:0]

Table 10-22. 0x21 - SHORT_ADDR_1

Bit	Field Name	Reset	R/W	Comments
7:0	SHORT_ADDR_1	0	R/W	Higher 8 bits of short address for address recognition, bits[15:8]

Table 10-23. 0x22 - PAN_ID_0

Bit	Field Name	Reset	R/W	Comments
7:0	PAN_ID_0	0	R/W	Lower 8 bits of PAN address for address recognition, bits[7:0]

Table 10-24. 0x23 - PAN_ID_1

Bit	Field Name	Reset	R/W	Comments
7:0	PAN_ID_1	0	R/W	Higher 8 bits of PAN address for address recognition, bits[15:8]

Table 10-25. 0x24 - IEEE_ADDR_0

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_0	0	R/W	Lower 8 bits of IEEE address for address recognition, bits[7:0]

Table 10-26. 0x25 - IEEE_ADDR_1

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_1	0	R/W	8 bits of IEEE address for address recognition, bits[15:8]

Table 10-27. 0x26 - IEEE_ADDR_2

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_2	0	R/W	8 bits of IEEE address for address recognition, bits[23:16]

Table 10-28. 0x27 - IEEE_ADDR_3

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_3	0	R/W	8 bits of IEEE address for address recognition, bits[31:24]

Table 10-29. 0x28 - IEEE_ADDR_4

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_4	0	R/W	8 bits of IEEE address for address recognition, bits[39:32]

Table 10-30. 0x29 - IEEE_ADDR_5

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_5	0	R/W	8 bits of IEEE address for address recognition, bits[47:40]

Table 10-31. 0x2A - IEEE_ADDR_6

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_6	0	R/W	8 bits of IEEE address for address recognition, bits[55:48]

Table 10-32. 0x2B - IEEE_ADDR_7

Bit	Field Name	Reset	R/W	Comments
7:0	IEEE_ADDR_7	0	R/W	Higher 8 bits of IEEE address for address recognition, bits[63:56]

Table 10-33. 0x2C - XAH_CTRL

Bit	Field Name	Reset	R/W	Comments
7:4	MAX_FRAME_RETRIES	3	R/W	Number of retransmission attempts in ARET mode before the transaction gets cancelled.
3:1	MAX_CSMA_RETRIES	4	R/W	Number of retries in ARET mode to repeat the CSMA-CA procedures before the ARET procedure gives up.
0		0	R/W	Reserved

Table 10-34. 0x2D - CSMA_SEED_0

Bit	Field Name	Reset	R/W	Comments
7:0	CSMA_SEED_0	234	R/W	Lower 8 bits of CSMA_SEED, bits[7:0] Seed for the random number generator in the CSMA-CA algorithm

Table 10-35. 0x2E - CSMA_SEED_1

Bit	Field Name	Reset	R/W	Comments
7:6	MIN_BE	3	R/W	Minimum back-off exponent in the CSMA-CA algorithm.
5		0	R/W	Reserved
4		0	R	Reserved
3	I_AM_COORD	0	R/W	Use for address filtering within RX_AACK states (PAN coordinator) 0: disable 1: enable For further details refer to IEEE 802.15.4-2003 section 7.5.6.2.
2:0	CSMA_SEED_1	2	R/W	Higher 3 bits of CSMA_SEED, bits[10:8] Seed for the random number generator in the CSMA-CA algorithm

11 Abbreviations

AACK	—	Auto acknowledge
ACK	—	Acknowledge
ADC	—	Analog-to-digital converter
AGC	—	Automatic gain control
ARET	—	Auto retry
AVREG	—	Analog voltage regulator
AWGN	—	Additive White Gaussian Noise
BATMON	—	Battery monitor
BBP	—	Base-band processor
BG	—	Band gap reference
CCA	—	Clear channel assessment
CRC	—	Cyclic redundancy check
CSMA	—	Carrier sense multiple access
DCLK	—	Digital clock
DCU	—	Delay calibration unit
DVREG	—	Digital voltage regulator
ED	—	Energy detection
ESD	—	Electro static discharge
EVM	—	Error vector magnitude
FCS	—	Frame Check Sequence
FCF	—	Frame Control Field
FIFO	—	First in first out
FTN	—	Automatic filter tuning
GPIO	—	General purpose input output
LDO	—	Low-drop output
LNA	—	Low-noise amplifier
LO	—	Local oscillator
LQI	—	Link-quality indication
LSB	—	Least significant bit
MAC	—	Medium access control
MFR	—	MAC Footer
MHR	—	MAC header
MSB	—	Most significant bit
MSDU	—	MAC service data unit
MSK	—	Minimum shift keying
O-QPSK	—	Offset-quadrature phase shift keying
PA	—	Power amplifier
PAN	—	Personal area network
PCB	—	Printed circuit board
PER	—	Packet error rate
PHY	—	Physical layer
PHR	—	PHY Header
PLL	—	Phase-locked loop
POR	—	Power-on reset
PPF	—	Poly-phase filter
PSDU	—	PHY service data unit
QFN	—	Quad flat no-lead package
RF	—	Radio frequency
RSSI	—	Received signal strength indicator
RX	—	Receiver
SFD	—	Start-of-frame delimiter
SHR	—	Synchronization Header

SPI	—	Serial peripheral interface
SRAM	—	Static random access memory
SSBF	—	Single side band filter
TX	—	Transmitter
VCO	—	Voltage controlled oscillator
VREG	—	Voltage regulator
XOSC	—	Crystal stabilized oscillator

12 Ordering Information

Ordering Code	Package	Voltage Range	Temperature Range
AT86RF230-ZU	QN	1.8V – 3.6V	Industrial (-40°C to 8 5°C) Lead-free/Halogen-free

Package Type	Description
QN	32QN1, 32-lead 5.0 x5.0mm Body, 0.50mm Pitch, Quad Flat No-lead Package (QFN) Sawn

Note: T&R quantity 4,000. Please contact your local Atmel sales office for more detailed ordering information and minimum quantities.

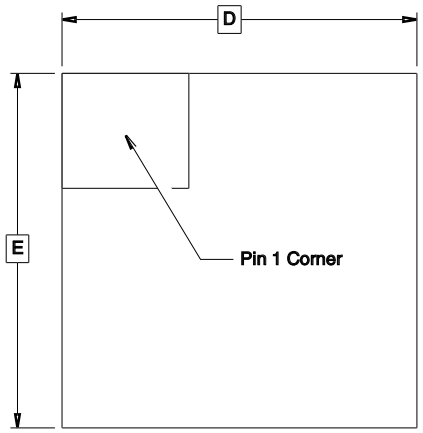
13 Soldering Information

Recommended soldering profile is specified in IPC/JEDEC J-STD-.020C.

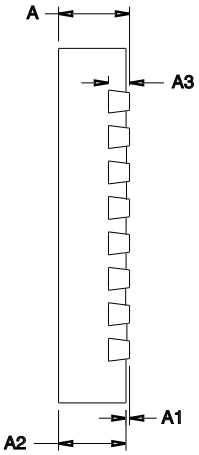
14 Package Thermal Properties

Thermal Resistance	
Velocity [m/s]	Theta ja [K/W]
0	40.9
1	35.7
2.5	32.0

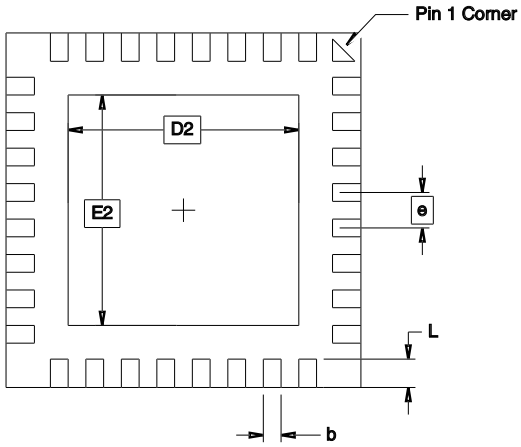
15 Package Drawing – 32QN1



Top View



Side View



Bottom View

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
D		5.00 BSC		
E		5.00 BSC		
D2	1.25		3.25	
E2	1.25		3.25	
A	0.80	0.90	1.00	
A1	0.0	0.02	0.05	
A2	0.0	0.65	1.00	
A3		0.20 REF		
L	0.30	0.40	0.50	
e		0.50 BSC		
b	0.18	0.23	0.30	2

Notes:
1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VHHD-1, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension should not be measured in that radius area.

1/24/06

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32QN1**, 32-lead 5.0 x 5.0 mm Body, 0.50 mm Pitch, Quad Flat No Lead Package (QFN) Sawn	32QN1	A

Appendix A - Continuous Transmission Test Mode

The Continuous Transmission Test Mode offers the following features:

- Continuous frame transmission
- Continuous wave signal transmission

A.1 - Overview

The AT86RF230 offers a Continuous Transmission Test Mode to support final application / production tests as well as certification tests. Using this test mode the radio transceiver transmits continuously a previously downloaded frame data (PRBS mode) or a continuous wave signal (CW mode).

In CW mode three different signal frequencies can be transmitted:

$f_1 = f_{CH}$ - 2 MHz

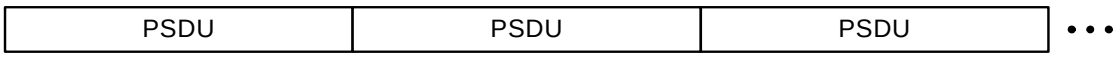
$f_2 = f_{CH}$ + 0.5 MHz

$f_3 = f_{CH}$ - 0.5 MHz

whereas f_{CH} is the center frequency of the current programmed cannel in register 0x08 (PHY_CC_CCA). Note, it is not possible to transmit a CW signal on the channel center frequency and to start a CW signal transmission without a previous download of valid data to the Frame Buffer (see sections 8.1 and 8.3).

In PRBS mode the transmission frequency is f_{CH}. Data downloaded to the Frame Buffer must contain at least a valid Frame Length Field (see sections 8.1 and 8.3). It is recommended to use a frame of maximum length (127 bytes) and arbitrary PSDU data. The SHR and the PHR are not transmitted. The transmission starts with the PSDU data and is repeated continuously (see **Figure A-1**).

Figure A-1. Frame Format in PRBS Mode



A.2 - Configuration

Before enabling the Continuous Transmission Test Mode (TST = 1) all register configurations shall be done as follows:

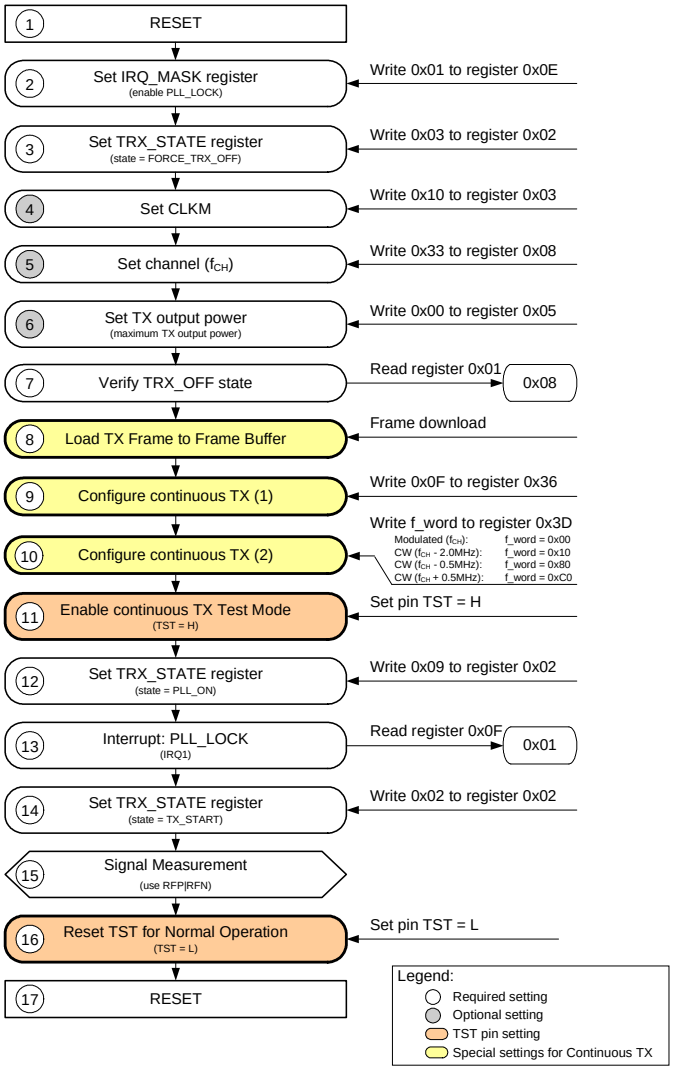
- Radio transceiver initialization (TRX_STATUS = TRX_OFF)
- TX channel setting (optional)
- TX output power setting (optional)
- Frame data download (random sequence of max. length)
- Mode selection (PRBS / CW)

Setting TST = H enables the Continuous Transmission Test Mode. The test system or a microcontroller has to overwrite the pull-down resistor R1 connected to the TST pin (see **Figure 5-1**). The pull-down resistor ensures a disabled test functionality during normal operation (TST = L).

The transmission is started by enabling the PLL (TRX_CMD = PLL_ON) and writing the TX_START command to register 0x02.

The detailed programming sequence is shown in **Figure A-2**.

Figure A-2. Programming Sequence - Continuous Transmission



A.3 - Disclaimer

The functionality of the Continuous Transmit Mode is not characterized by Atmel and therefore not guaranteed.

The normal operation of the AT86RF230 is only guaranteed if pin TST is always logic low.

Appendix B - Errata

AT86RF230 Rev. A

B.1 - Data frames with destination address=0xFFFF is acknowledged in RX_AACK

According to IEEE 802.15.4-2003 data frames with destination address=0xFFFF (broadcast) should not have the acknowledgment request subfield set in the frame control field. If such a non-standard compliant data frame arrives, a device in RX_AACK state acknowledges that frame.

Problem Fix/Workaround

Use only standard compliant frames, i.e. do not initiate frames with destination address=0xFFFF (broadcast) and the acknowledgment request subfield set.

B.2 - Frame upload in RX_AACK

The following frames are not uploaded:

(1) Data frames and command frames with destination PAN ID=0xFFFF and extended destination addressing mode

(2) Beacon frames, when the PAN ID of the receiving node is set to 0xFFFF.

Problem Fix/Workaround

(1) Use Basic Operating Mode for orphan scanning

(2) Use Basic Operating Mode for network scanning

B.3 - TX_ARET returns TRAC_STATUS=SUCCESS even though transaction failed

It might happen that under very special conditions (e.g. noisy network environment) the status bit TRAC_STATUS (register 0x02) after transmission of a frame is SUCCESS even though the transaction failed.

Example

A node transmits a frame with the acknowledgment request subfield set to 1 and waits for an incoming ACK. If no frame is received at the end of the ACK wait period (54 symbols), but a valid preamble is detected (e.g. jammer/interferer signal), the TX_ARET procedure is finished immediately. A TRX_END interrupt is generated. The TRAC_STATUS is not updated and thus shows the default value SUCCESS.

Problem Fix/Workaround

The workaround comprises two changes:

1. Set variable MAX_FRAME_RETRIES to 0. This prevents any retransmissions of the TX_ARET procedure and has to be implemented in S/W. A retransmission does not require a frame download again, only TX_START command is necessary.
2. Control of the TX_ARET procedure should follow these steps:
   - TRX_STATUS == TX_ARET_ON
   - set TRX_CMD = TX_START and download frame
   - poll for TRX_STATUS == BUSY_TX_ARET
   - set TRX_CMD = RX_ON
   - wait for TRX_END IRQ

- read TRAC_STATUS
- set TRX_CMD = TX_ARET_ON
- poll for TRX_STATUS == TX_ARET_ON

Switching to RX_ON is not executed during BUSY_TX_ARET but immediately after BUSY_TX_ARET has completed. This enables the receiver to receive a frame which arrives shortly before the end of the ACK wait period. In this case TRAC_STATUS is not accidentally set to SUCCESS and is still correct (NO_ACK), as long as the frame is received. That means the software has additional time to read the TRAC_STATUS.

Using the workaround mentioned above, the failure occurrence is considerably reduced. A wrong TRAC_STATUS can still be observed, but very seldom (one of million transmissions).

B.4 - Sensitivity to continuous wave interferers

Due to the high receiver sensitivity continuous wave interferers may cause RX_START interrupts. This may result in missed frames since the receiver is kept busy detecting preambles and SFD. One cause of continuous wave interferers may be due to crosstalk from clock.

Problem Fix/Workaround

For further details see application note AVR2005 "AT86RF230 - Hardware Design Considerations".

B.5 - TRX_END_IRQ occurs sometimes too late in TX_ARET_ON state

This behavior can be observed, if the procedure TX_ARET performs frame retransmissions.

Problem Fix/Workaround

Set register bit MAX_FRAME_RETRIES = 0 (register 0x2C) and implement frame retries by software. A frame retransmission does not require downloading the frame again, only TX_START command is necessary.

B.6 - TX_ARET ACK wait time too short

The maximum number of symbols waiting for an acknowledgment frame should be 54 symbols as defined in IEEE 802.15.4-2003. The implemented waiting time is 46 symbols.

Problem Fix/Workaround

None

B.7 - CCA Request is not executed

A requested CCA may be rejected without execution. In this case the CCA_DONE bit indicates “CCA calculation in progress” even though the calculation must be finished already.

Problem Fix/Workaround

The TRX_STATUS is RX_ON. To initiate a CCA request, switch to PLL_ON state and back to RX_ON state. Immediately after the state change initiate a CCA request. It is not necessary to confirm the state changes.

References

[1] IEEE Std 802.15.4-2003: Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)
[2] ANSI / ESD-STM5.1-2001: ESD Association Standard Test Method for electrostatic discharge sensitivity testing – Human Body Model (HBM)
[3] ESD-STM5.3.1-1999: ESD Association Standard Test Method for electrostatic discharge sensitivity testing – Charged Device Model (CDM)

Revision History

Rev. 5131C-ZIGB-05/22/07

1. Major revise of sections 1 to 10
2. Added “Appendix A - Continuous Transmission Test Mode”
3. Added “Appendix B - Errata”

Rev. 5131A-ZIGB-06/14/06

1. Initial release

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